

A Compact 2.4V Power-efficient Rail-to-rail Operational Amplifier

Abstract

Strong inversion operation stops a proposed compact 3V power-efficient rail-to-rail Op-Amp from a lower total supply voltage. By biasing some critical transistors into weak inversion region, the minimum supply voltage successfully dropped below 2.4V. Skilful utilizing the large transconductance of weak inversion operation also led to much better specifications, such as the DC gain, than the original 3V Op-Amp. The 2.4V Op-amp attains a DC gain of 110dB, an unit-gain frequency of 1MHz, slew rate of 9.7V/ μ s, and bandwidth-power ratio of 9.3MHz/mW, as the load capacitance equals 10pF and the load resistance equals 1M Ω .

I. Introduction

Low-voltage low-power systems have received increasing interests. Operational amplifier (Op-amp) is the basic element of analog circuit; the design of low-voltage Op-amp is thereby the fundamental work of designing low-voltage analog systems. A compact 3V rail-to-rail Op-amp has been implemented in [1]. The word compact refers to efficient power consumption, small layout area and the compatibility with digital circuits. Strong inversion operation in the whole circuit requires a minimum supply voltage above 3V. Although rail-to-rail Op-amps that run on supply voltages below 2V were also implemented in [2]-[4], the output of [2] and [3] doesn't critically swing from rail-to-rail because of the cascoded output stage. Reference [4] utilizes a class-AB output stage, but doesn't include the class-AB control circuit. The power supply rejection of [4] is thus worse.

MOS transistor in weak inversion operation has a gate-source voltage smaller than the threshold voltage, as well as a much larger transconductance due to the

exponential current-voltage relationship; therefore, we directly operated several transistors of [1] into weak inversion region to obtain a compact Op-amp with minimum supply voltage below 2.4V. The matching and noise property of weak inversion operation, however, becomes worse. Careful selection of transistors in weak inversion operation is thereby important. Section 2 discusses the selection of suitable transistors in the rail-to-rail input stage, while the selection of suitable transistors in output stage is left in section 3. Section 3 reveals the measuring results. The final section concludes the contribution.

II. Design of the rail-to-rail input stage

Paralleling an N-channel and a P-channel input pair allows a common mode input range from rail to rail [5]. Such complementary input pairs, however, confine the Op-amp's attainable minimum supply voltage to two gate-source voltage plus two saturation voltage [6]. Figure 1 displays the rail-to-rail input stage in our design. We biased the complementary input pairs, M11-M14, into weak inversion region, instead of saturation region, to release the confinement above. The fabricating process is the 0.8um 1P3M n-well CMOS process offered by TSMC. Typical values of The threshold voltage for NMOS and PMOS transistors are 815mV and 895mV. The variation may reach about 15%. The gate-source voltage of M11-M14 are 100mV lower than the threshold voltage in our design. Let the minimum saturation voltage, required by current source, be 200mV. The total supply voltage can be lower than 2.4V.

Let I_p , I_n , n_n and n_p be the bias current and slope factor of NMOS and PMOS transistor in weak inversion region respectively. The total input transconductance, g_m , equals to

$$g_m = \frac{I_p}{n_p V_{th}} + \frac{I_n}{n_n V_{th}} \quad (1)$$

where V_{th} is the thermal voltage, kT/q . Optimal frequency compensation requires input transconductance to be constant over entire common-mode input range; thereby, a constant- g_m control circuit is necessary. The one-time current mirror [5], M15-M17, fulfills our requirement, instead of the three-times current mirror of [1].

Equation (1) implies that the difference between n_n and n_p induces a variation of total transconductance. Modifying the gain factor of one-time current mirror can largely compensate such variation. The W over L ratio of M17 is thus slightly larger than that of M16. Simulating maximum variation is only 4%.

Transistors M1-M5 mirror the reference current to the current source, M10, of PMOS input pair. M15-M17 gradually switch the bias current to NMOS input pair when input common-mode voltage exceeds the gate-voltage of M15. To maximize the common-mode rejection ratio, the W over L ratio of M15 has to be small compared to the input transistor [5]. But note that M10 would enter linear region if the W over L ratio of M15 is too small. Transistor M10d and M17d, which are connected with M10 and M17 in parallel, facilitates the measurement of bias current for both PMOS and NMOS input pairs.

III. Design of rail-to-rail output stage

Figure 2 displays the rail-to-rail class-AB output stage in our design. The class-AB control circuit, M32 and M36, is shifted into the summing circuit, M21-M28. Such clever design makes the Op-amp deserves the word *compact* [1]. The floating current source, M43 and M46, biases the summing circuit. Although the output stage requires one saturation voltage less than input stage for minimum supply voltage, the body effect of M32, M33 and M43 drastically elevates their threshold voltage to more

than 1.1V. Were all transistors biased in strong inversion region, such a high threshold voltage would force transistor M30 into linear region when total supply voltage is lower than 2.5V. To enhance further lowering of total supply voltage, we biased M32, M33 and M43 into weak inversion region. For symmetry, transistors M36, M38 and M46 are also biased in weak inversion region. The bias current of the floating current source is then given by

$$I_{bias} = 2I_{M30} \frac{\left(\frac{W}{L}\right)_{27}}{\left(\frac{W}{L}\right)_{34}} \quad (2)$$

where I_{M30} is the drain current of M30 and equals to 3uA.

Operating class-AB output transistors, M31 and M35, in weak inversion region is somewhat impractical. The quiescent current of the output transistor is normally larger than that of input transistor, in order to enhance the driving capability of the Op-amp. A much larger W over L ratio is then necessary for ensuring the output transistor in weak inversion region. In addition, the allowable swing range of the gate-voltage of the output transistor is also limited to avoid entering strong inversion operation. Such limitation degrades the maximum output current of the Op-amp; therefore, the output transistors are still biased in strong inversion region. The quiescent current is written as the following equation, similar to equation (2).

$$I_q = 2I_{M30} \frac{\left(\frac{W}{L}\right)_{31}}{\left(\frac{W}{L}\right)_{34}} \quad (3)$$

Transistors M31-M34 in figure 2 are connected as the feedback capacitors. The frequency compensation of the Op-amp is achieved by nested cascoded miller compensation [5]. CM3 and CM4 improves the high frequency behavior of the Op-amp, while capacitors CM1 and CM2 tame the damped oscillations in transient response. After adjustment, CM3 and CM4 are set at 1.5pF, CM1 and CM2 at 0.5pF.

IV. Measurement results

Figure 3a shows the measured bias current of P-channel and N-channel input pairs when input common-mode-voltage, V_{cm} , sweeps from rail to rail. This figure reveals that the constant- g_m control circuit functions properly. The control circuit starts to switch bias current from P-channel into N-channel input pair when V_{cm} increase beyond 1.2V. Both input pairs share the bias current at $V_{cm}=1.4V$, while N-channel input pair takes all tail current as V_{cm} is larger than 1.6V. To confirms the rail-to-rail operation of the Op-amp, the Op-amp is connected as a unit-gain buffer with positive input sweeping from rail to rail. The measured output signal, as displayed in figure 3b, sincerely follows the positive input signal over the entire common-mode voltage. The CMRR over the entire common-mode voltage are also deduced from figure 3b by the following equation

$$CMRR = \frac{\Delta V_{common}}{\Delta V_{os}} \quad (4)$$

Figure 4 displays the measured frequency response of the Op-amp. The unit-gain bandwidth is 1MHz with phase margin of 72° . Extrapolating the data gives that the gain of the Op-amp is 110dB at 10Hz. Figure 5 plots the measured unit-gain bandwidths versus different input common-mode voltage. The maximum variation is 8%, larger than the simulating variation of total input conductance, 5%. We attributed such a little larger variation to that a gate-source voltage of 100mV below the threshold voltage might not be enough to force the MOS transistor deeply into the weak inversion operation. The current-voltage relationship of the MOS transistor slightly deviates from the exponential model; therefore, the constant- g_m control circuit was not as effective as our anticipation.

Table 1 summarizes the measured specification of the Op-amp. The measured low-frequency gain is 23dB more than that of the Op-amp in [1]. Figure 7 shows the

output waveform of the step response. The slew rate is 9.5V/us at the rising edge and 4.9V/us at the falling edge when the load capacitance equals 10pF. The values of slew rate and input noise are also better. All the improvement is attributed to the large transconductance of weak inversion operation. Such large transconductance straightly enhance the overall gain, as well as small signal response of the Op-amp.

V. Conclusion

Skilful use of weak inversion operation successfully lead to a 2.4V compact Op-amp. The attainable minimum operating voltage is only 2.2V, as indicated in Table 1. The bandwidth-power ratio is as high as 9.3MHz/mW while the layout area is only 0.07mm². Comparing to the specification of the Op-amp in [1], the performance of the our Op-amp doesn't degrade with weak inversion operation. On the contrary, the large transconductance of weak inversion operation contributes to larger low-frequency gain and higher slew rate. Such result confirms the application of weak inversion operation in other low-voltage low-power circuits.

Reference

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- [6] Ron Hogervorst and Johan H. Huijsing, “Design of Low-voltage Low-power Operational Amplifier Cells,” *Kluwer Academic Publishers*, 1996.

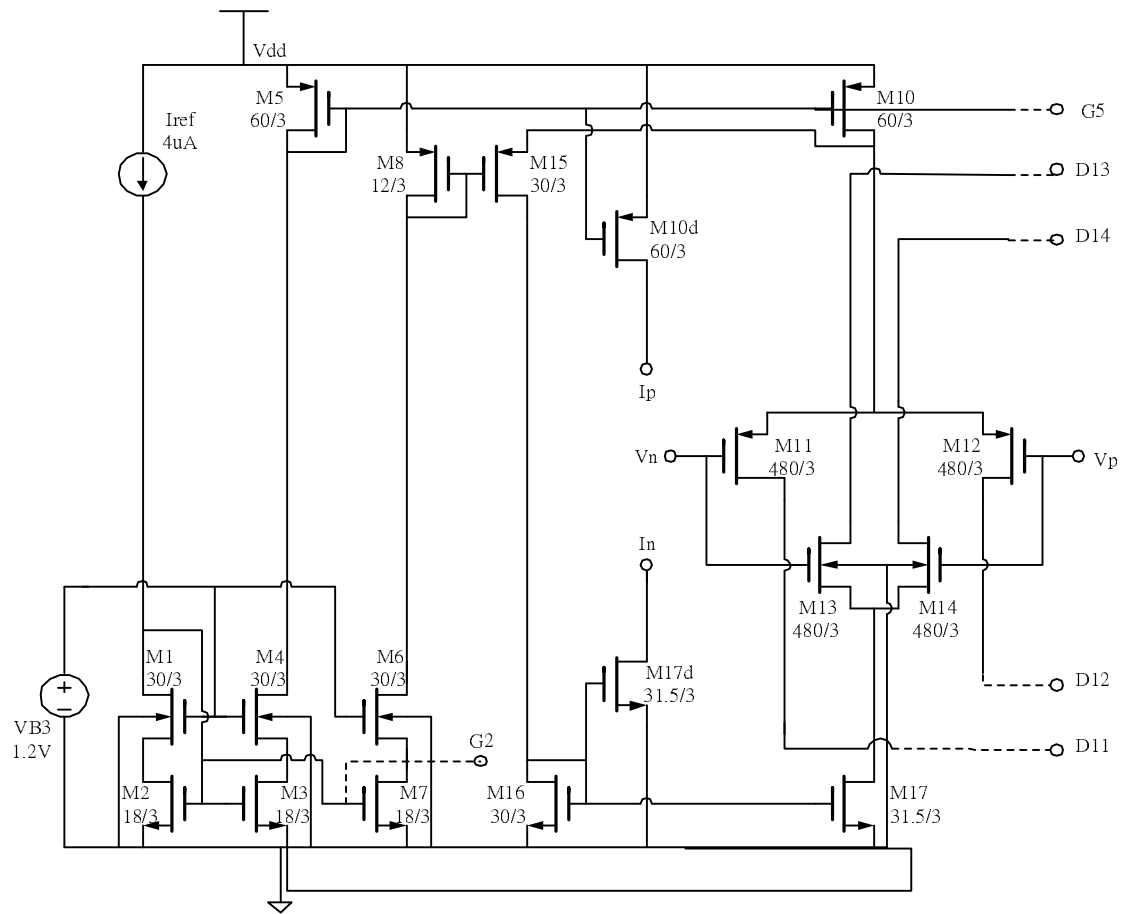


Figure 1 The rail-to-rail input stage in our design

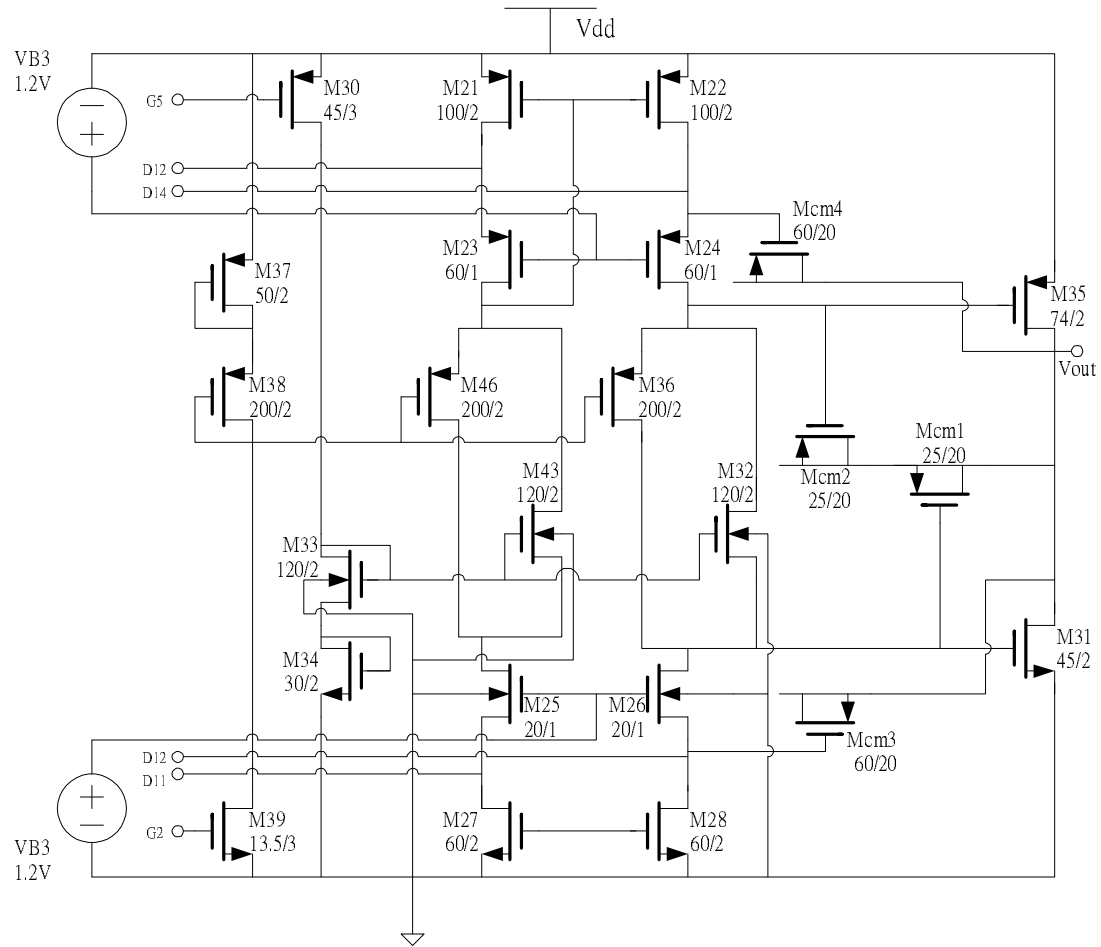


Figure 2 The rail-to-rail output stage in our design

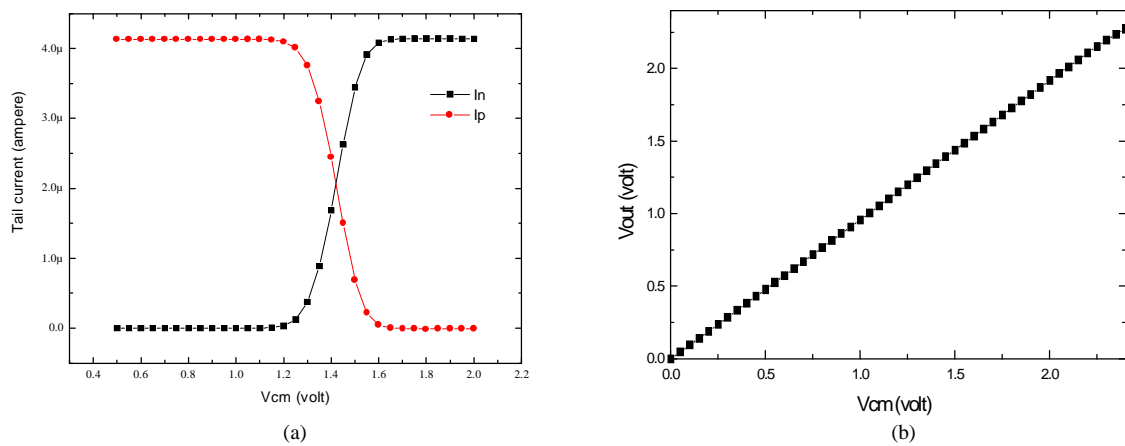


Figure 3 (a) The tail current of the P-channel and N-channel input pair (b) The rail-to-rail output signal when the common mode voltage seeps from rail to rail

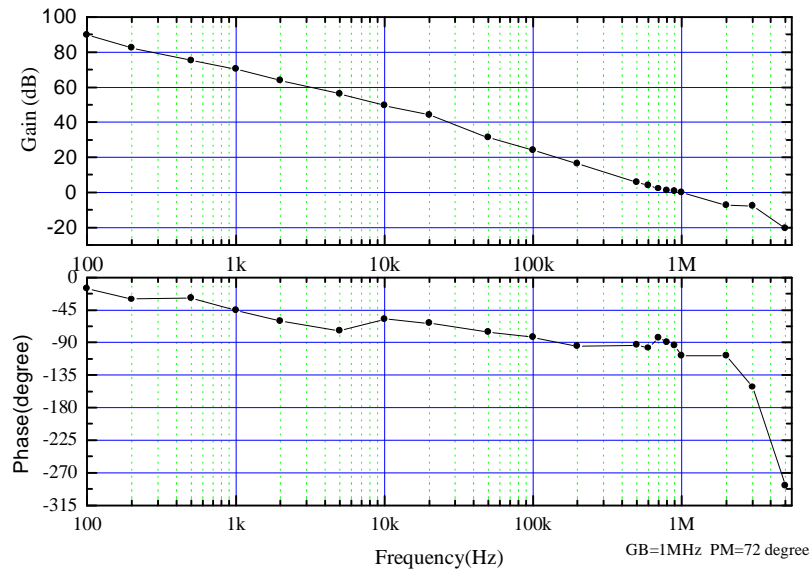


Figure 4 The frequency response of the Op-amp

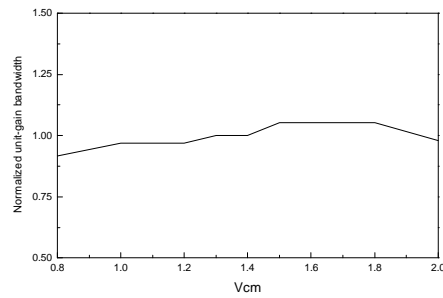


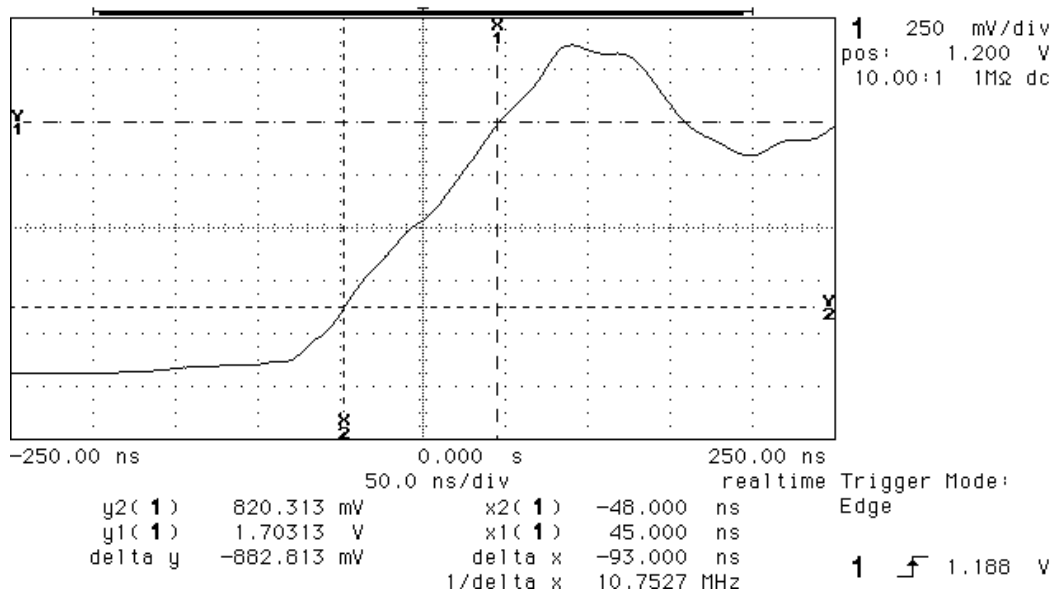
Figure 5 Normalized unit-gain bandwidth versus the common-mode voltage

Table 1 The measured specifications of the 2.4V rail-to-rail Op-amp

PARAMETER		VALUE	UNIT
Process		0.6 um n-well CMOS 1P3M	
Layout area		0.07	mm^2
Supply voltage range		2.2~5.0	V
Quiescent current		44.8	μA
V_{CM} range		$V_{SS} - 0.5$ to $V_{DD} + 0.4$	V
V_{OUT} range		$V_{SS} + 0.05$ to $V_{DD} - 0.05$	V
CMRR	$V_{CM} < 1.2$ or $V_{CM} > 1.6$	80	dB
	$1.2 < V_{CM} < 1.6$	49.5	dB
Offset voltage (V_{os})		2.55	mV
Input noise (I_{noise}) at 100Hz		233+	nV/\sqrt{Hz}
Low-frequency gain		110	dB
Unit-gain bandwidth		1	MHz
Phase margin		72	Degree

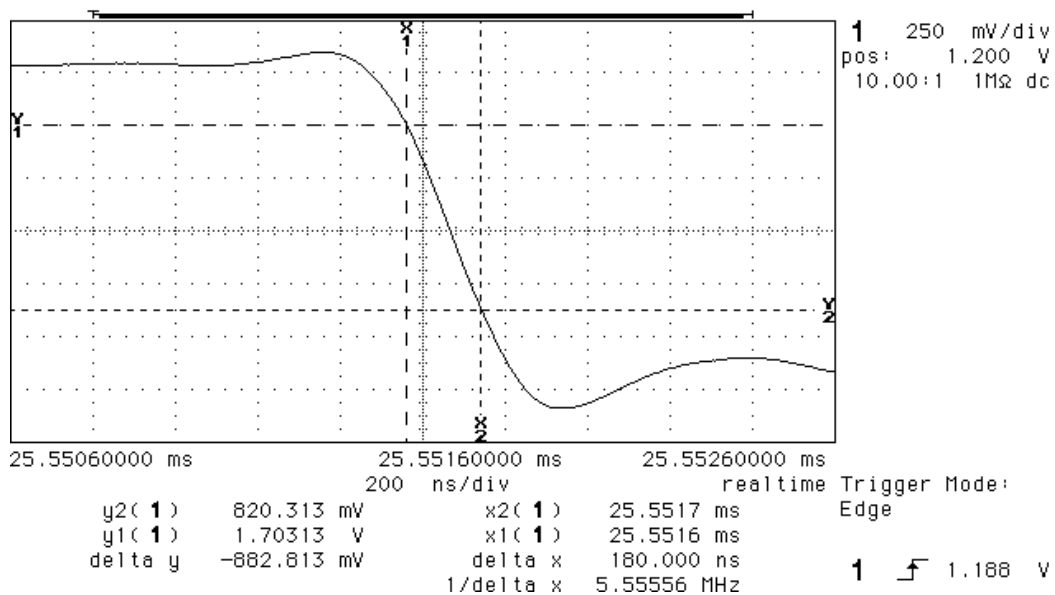
Slew rate	CL=10pF	SR+ = 9.5, SR- =4.9	V/ μ s
Bandwidth-power ratio (F_M)		9.3	
$V_{sup\ ply} = 2.4V, R_L = 1M\Omega, C_L = 10pF$			

hp



(a) rising edge

hp stopped



(b) falling edge

Figure 7 Step-response waveform, $SR = (\Delta y)/(\Delta x)$