2V Operational Amplifiers with Rail-to-Rail Input and Output Ranges

Abstract

Two 2V operational amplifiers (Op-amp) with rail-to-rail input and output ranges were implemented. The regulated cascoded current mirrors and the feedback class-AB controlled output stage are used to allow further lowering of operating voltage. The first Op-amp had an unit-gain bandwidth of 4.8MHz and DC gain of 130dB. The second Op-amp employed the multi-path-driven technique to attain a higher unit-gain bandwidth of 6.6MHz with DC gain of 135dB. Both Op-amps, compared to all other proposed Op-amps, are the most power-efficient design.

I. Introduction

Low-voltage low-power Op-amp is the basic element of low-voltage low-power circuits. Reference [1] already implemented a compact power-efficient 3V rail-to-rail Op-amp mainly by combining the summing circuit with feedforward class-AB controlled circuits; however, too many cascoded transistors in the summing circuits stops further lowering of the operating voltage. Rail-to-rail Op-amps with modified architecture that run on supply voltages lower than 2V were implemented in [2]-[4]. But the output of [2] and [3] doesn't critically swing from rail-to-rail because of the cascoded output stage. Reference [4] employees a class-AB output stage without class-AB control circuit. The power supply rejection of [4] is therefore worse.

Two 2V rail-to-rail Op-amps are realized in this thesis. The regulated cascoded current mirrors (RGC) [5], as suggested by [2], form the summing circuit in the input stage. As for the output stage, the feedback class-AB controlled circuit [6] is included. The second Op-amp then employees the multi-path-driven technique [7] to attains a better high-frequency performance. Section 2 discusses the design of input stage. The design of output stage is discussed in section 3. Section 4 deals with the frequency compensation and introduces the multi-path-driven technique. The measurement results are presented in section 5. The final section concludes the achievement and look into the future.

II. Design of rail-to-rail input stage

Figure 1 displays the rail-to-rail input stage in our design. The complementary

input pairs, M11-M14, enable the Op-amp to manage common-mode input signal from rail to rail [8]. But a minimum supply voltage of two gate-source voltages plus two saturation voltages is required by the complementary input pair [1]. To release this confinement, the complementary input pair is biased into weak inversion region, instead of strong inversion region. The constant-g_m controlled circuit therefore employees the one-time current mirror, M15-M17, to facilitate the frequency compensation of the Op-amp [6]. The fabricating process is 0.8um n-well CMOS process offerred by TSMC. Typical values of the threshold voltage for NMOS and PMOS transistors are 815mV and 895 mV. The normal operation of the complementary input pair thus only requires a supply voltage larger than 1.8V in our design.

Merging the summing circuit with the feedforward class-AB controlled circuit, reference [1] successfully implemented a 3V power-efficient Op-amp with small layout area. The removal of too many cascoded circuits in the summing circuit, however, is necessary if the operating voltage is less than 2V. The improved summing circuit, as circled by the dashed line in figure 1, consists of the subcircuit of the regulated cascoded current mirrors (RGC) [5]. Each group of two cascoded NMOS transistors represents the subcircuit in figure 2a; similarly, each group of two cascoded PMOS transistors corresponds to the subcircuit in figure 2b. Basic operating principle of the RGC circuit is utilizing the feedback transistors, Mnr3 and Mpr3, to keep the drain potential of the input transistors, Mnr1 or Mpr1, constant. The composite transistors, Mnr1-Mnr2 or Mpr1-Mpr2, than behave like a “super transistor that has a large output resistance of

$$r_o = \frac{g_{m2} g_{m3}}{g_{ds1} g_{ds2} \left(g_{ds3} + g_{ds5} \right)} \tag{1}$$

where g_{ds1}-g_{ds5} are the channel conductance of transistor M1-M5 and g_{m2}-g_{m3} are the transconductance of transistors M2-M3. Such a large output resistance not only enlarges the output swing range of the summing circuit, but also increases the overall gain of the Op-amp.

III. Design of rail-to-rail output stage

The rail-to-rail output stage requires the push-and-pull output transistors

connected in common-source configuration [8]. A class-AB controlled circuit is then necessary, in order to achieve a good comprise between distortion and quiescent dissipation. Figure 3 displays the rail-to-rail output stage with the feedback class-AB controlled circuit [9] in our design. The output stage requires a minimum supply voltage of only one gate-source voltage plus one saturation voltage. Two common-source gain stages, M31-M32, split the output of the summing circuit into two in-phase signals for the output transistors, Mop and Mon. Transistors M46 and M44 sense the drain currents of the output transistors. The voltage drops of the folded diodes, M41 and M43, then represent the drain current of Mon and Mop respectively. The differential amplifier, M51-M53, compares the reference voltage, set by M36, to the drain voltage of the folded diodes. Differential signals would be fed back into the gates of output transistors through M47-M50, as long as the drain voltage of the folded diodes is different from the reference voltage.

As an example, pushing the in-phase signals into the output transistors induces a large drain current through Mon, as well as a lower current through Mop. The voltage drops of M43 is then much larger than M41 and M36. As sensing the differential signal, the feedback amplifier pulls a current from the gate of Mop and push an equal amount into the gate of Mon. Transistor Mop are then kept from turning off when Mon is pulling an increasing current from the load. <<Figure 4a displays the simulating drain currents of the output transistors when input common-mode voltage sweeps from rail-to-rail. The change of gate voltages of the output transistors is shown in figure 4b. It is obvious that the feedback class-AB controlled circuit sets a maximum value for the gate voltage of Mop, while a minimum value for the gate of Mon.>>

IV. Frequency compensation and multi-path-driven technique

Frequency compensation of the 2V Op-amp is achieved by the nested Miller compensation [6]. Transistors Mcm1-Mcm2 in figure 3 function as the Miller capacitors for the inner Miller loop, while the outer Miller loop requires an additional capacitor CM3, connected between the drain of the output transistor and the output of the summing circuit. After adjustment, we set CM1=CM2=0.5pF and CM3=1.2pF. The simulating frequency response of the Op-amp is shown in figure 5. The Op-amp has a unit-gain bandwidth of 4.8MHz and phase margin of 62° when R_L=1MΩ and

C_L=10pF. Such unit-gain bandwidth, as well as phase margin, is not better enough owing to the cascaded output stage. Another 2V Op-amp thus employee the multi-path-driven technique [7] to enhance the high frequency response.

Figure 6 displays the modified part of the new Op-amp, including the complementary input pairs, summing circuits and the common-sourse gain stages. The current mirrors, Xpr1-Xpr5 and Xnr1-Xnr5, still refer to the RGC subcircuits in figure 2. The in-phase outputs, Gon and Gop, of the common-source gain stages are fed to the feedback class-AB controlled output stage. Each input transistor is divided into three parts. Mxxc and Mxxd have equal channel width while Mxxab and Mxxcd have two times channel width of Mxxc and Mxxd. Note that the sum of the channel width of three related transistors equals the channel width of original input transistor in figure 1. there are two paths from the input pairs to the drain of common-source gain stage. The first path passes through the complementary input pairs M11ab-M14ab and M11cd-M14cd, the summing circuit Xpr1-Xpr2 and Xnr1-Xnr2, and the common-source amplifiers. The second path composes of the remaining input transistors and summing circuits. As indicated by the two bode line in figure 6, the second path skips the common-source gain stages and links to the output transistors directly. The high-frequency input signal can thus reach the output stage through the second path while the first path still maintains a high gain of the low-frequency input signals. The simulating frequency response of the improved Op-amp is shown in figure 7. The unit-gain bandwidth is 6.65MHz and the phase margin is $55^\circ$when R_L=1MΩ and C_L=10pF.

V. Measurement results

Transistors M10d and M17d, connected with M10 and M17 in parallel in figure 1, facilitates the measurements of bias current for both PMOS and NMOS input pairs. Figure 8a shows the measured bias current of the complementary input pairs when the input common-mode voltage (V_{CM}) sweeps from rail-to-rail. The one-time current mirror starts to switch the bias current from P-channel into N-channel input pair when V_{CM} increase beyond 0.8V. Both input pairs share the total bias current at V_{CM}=1V, while N-channel input pair takes all current as V_{CM} exceeds 1.2V. The function of the constant-g_m control circuit is thus prove valid. With the Op-amp connected as a

unit-gain buffer, the measured output signal is displayed in figure 8b when the positive input sweeps from rail to rail. This figure confirms the rail-to-rail operation of the 2V Op-amps. The CMRR over entire V_{CM} ranges can be also deduced from this measurement according to the following equation

$$CMRR = \frac{\Delta V_{common}}{\Delta V_{os}} \tag{2}$$

The maximum CMRR of the first Op-amp (20OP1) is 65dB, while that of the second Op-amp (20OP2) is only 44dB. We attributed such degradation to the complicated division of the complementary input pairs of 20OP2. Such division cause worse matching between input transistors, as well as current mirror loads; therefore, the denominator in equation (2) becomes even larger for 20OP2. The 2V Op-amps' output waveforms of the step response are shown in figure 10. The slew rate of 20OP2 is nearly two-times larger than that of 20OP1. The multi-path-driven configuration contributes to such improvement. Table 1 summarizes the measuring specifications of two rail-to-rail Op-amps.

Figure 10 plots bandwidth versus minimum supply voltage of our Op-amps, as well as that of the proposed Op-amps in the references. The circular marks represent the CMOS Op-amps while the up-triangle marks represent Op-amps fabricated with bipolar process. Filled circular marks refer to the CMOS rail-to-rail Op-amp implemented in the thesis. Remind that lower supply voltage and power lead to lower maximum bandwidth attainable; therefore, the closer to the left-up corner the mark is, the more power-efficient design the corresponding Op-amp is. Bipolar transistors have smaller turn-on voltage and saturation voltage. But the maximum attainable bandwidth of bipolar Op-amps is 4MHz [8]; therefore, bipolar Op-amps concentrate in the left-down corner Although the Op-amp of [2] seems to have best performance, the architecture of the Op-amp doesn't include the class-AB output stage. In addition, only simulating results are presented in [2]. As an obvious consequence, figure 10 reveals that the Op-amps implemented in the thesis attains lowest operating voltage and highest bandwidth than all the other CMOS Op-amps. i.e. The Op-amps are the most power-efficient design.

VI. Conclusions

Combining RGC summing circuits and feedback class-AB controlled output stages, we successfully implemented the 2V Op-amps that really have rail-to-rail input and output ranges. With the multi-path-driven technique, the Op-amp achieves a most power-efficient design with bandwidth of 135dB and power dissipation of 632uW only. If the operating voltage of the Op-amp is going to be below 1.5V, chief limitations again occurs in the complementary input pairs Two methods can resolve this problems. One of the methods is operating the input pairs in the lateral bipolar mode [10] because the turn-on voltage of the transistor is only 0.5-0.7V in this mode; however, twin-well CMOS process is necessary. The other method is utilizing the level shifter [11]. the only payment is lots of layout area for the level-shift resistors.

References

[1] Ron Hogervorst, John P.Tero, Ruud G. H. Eschauzier, and Johan H. Huijsing, "A Compact Power-efficient 3V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries," *IEEE journal of Solid-State Circuits*, Vol. 29, No. 12, December 1994.

[2] Abdulkerim L. Coban and Phillip E. Allen, "A 1.75V Rail-to-Rail CMOS Op-Amp," *Proceedings of the IEEE International Symposium on Circuits and Systems*, 1994.

[3] S. Setty and C. Toumazou, "CMOS +1V to –1V Rail-to-Rail Operational Amplifier," *The International of Electrical Engineers*, 1994.

[4] Giuseppe Ferri, and Willy Sansen, "A 1.3V Op-amp in Standard CMOS with Constant-g_m and Rail-to-Rail Input and Output Stages," *1996 IEEE International Solid-State Circuits Conference*, ISSCC96, February 10, 1996.

[5] P. J Crawley and G. W. Roberts, "High-Swing MOS Current Mirror with Arbitrarily High Output Resistance," Electronics Letters, Vol. 28, No. 4, February 1992.

[6] Ron Hogervorst and Johan H. Huijsing, "Design of Low-voltage Low-power Operational Amplifier Cells," *Kluwer Academic Publishers*, 1996.

[7] Jeroen Fonderie and Johan H. Huijsing, "Operational Amplifier with 1V Rail-to-Rail Multi-path-driven Output Stage," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 12, December 1991.

[8] Johan H. Huijsing and Daniel Linebarger, "low-Voltage Operational Amplifier with Rail-to-Rail Input and Output Ranges," *IEEE journal of Solid-State Circuits*, Vol. SC-20, No. 6, December 1985.

[9] R.G.H. Eschauzier, R. Hogervorst, J.H. Huijsing, “A Programmable 1.5V CMOS Class-AB Operational Amplifier with Hybrid Nested Miller Compensation for 120dB Gain and 6 MHz UGF”, *IEEE journal of Solid-State Circuits*, vol. SC-29, no. 12, December 1994, pp. 1497-1504.

[10] Eric A. Vittoz, “MOS Transistors Operated in the Lateral Bipolar Mode and Their Application in CMOS Technology,” IEEE Journal of Solid-State Circuits, Vol. Sc-18, No. 3, June 1983.

[11] Jeroen Fonderie, Marinus M. Maris, Erik J. Schnitger, and Johan H. Huijsing, “1-V Operational amplifier with Rail-to-Rail Input and Output Ranges,” *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 6, December 1989.

Table 1 The measured specifications of the 2V rail-to-rail Op-amps

PARAMETER		20OP1	20OP2	UNIT
Supply voltage range		1.8~5.0	1.8~5.0	*V*
Quiescent current		245	316	μA
V_{CM} range		$V_{SS}-0.5$ to $V_{DD}+0.4$		*V*
V_{OUT} range		$V_{SS}+0.05$ to $V_{DD}-0.05$		*V*
CMRR	V_{CM}<0.8 or V_{CM}>1.2	67	44	*dB*
	0.8<V_{CM}<1.2	43	30	*dB*
Offset voltage (V_{OS})		8.9	65.4	*mV*
Low-frequency gain		130 (sim)	133 (sim)	*dB*
Unit-gain bandwidth		4.8 (sim)	6.6 (sim)	*MHz*
Phase margin		62 (sim)	55 (sim)	*Degree*
Slew rate (CL=10pF)		SR+ =33, SR-=13	SR+ = 57, SR-=24	$V/\mu s$
Test condition		$V_{supplly}$=2.0V, V_{CM}=1.0V, R_L=1MΩ, C_L=10pF		