High Voltage Lateral 4H-SiC JFETs on a Semi-insulating Substrate

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Outline

- Introduction
- Concept and Design
- Fabrication Process
- Results
- Summary

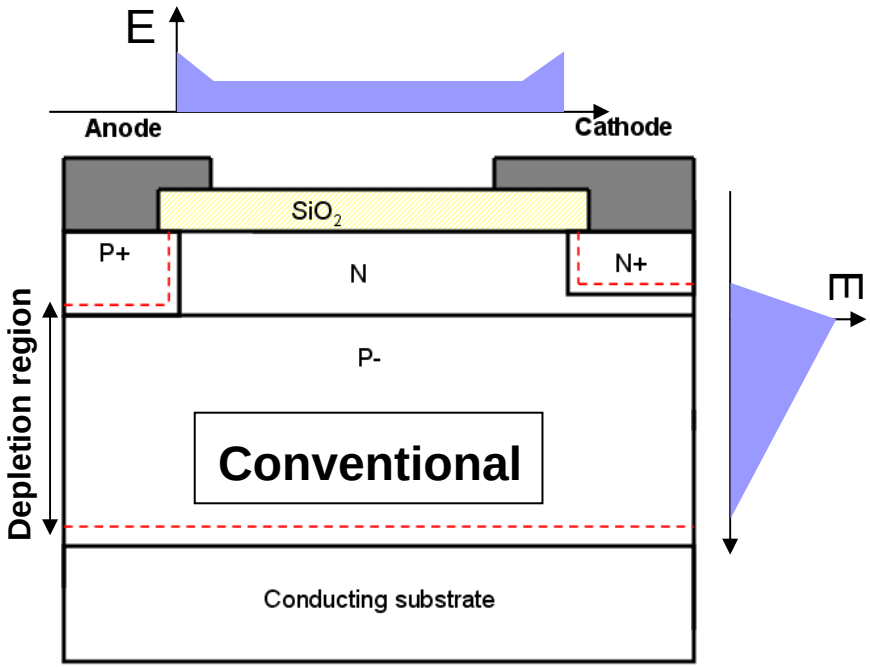
Introduction

- 4H-SiC power devices have shown promising performance due to superior material properties (E_g = 3.24 eV, E_c= 2-4E6 V/cm, k = 4.9 W/cmK).
- Lateral devices have the advantage of being integrated with other devices.
- 4H-SiC lateral devices have broken through the limit of Si vertical devices.
  - 1000 V, 9.2 mΩ-cm^2 4H-SiC lateral JFET

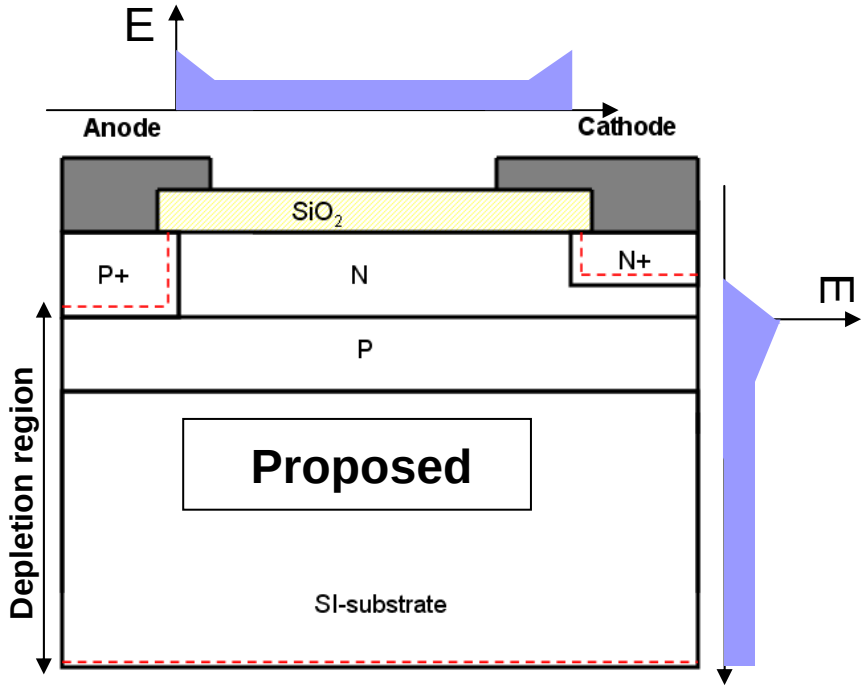
    (Y. Zhang et al., *IEEE Electron Device Letters,* **28**, 404-407, 2007)
  - 1380 V, 66 mΩ-cm^2 4H-SiC lateral MOSFET

    (M. Noborio et al., *IEEE Trans. Electron Devices*, **54**, 1216-1223, 2007)

Conventional vs. Proposed Approach



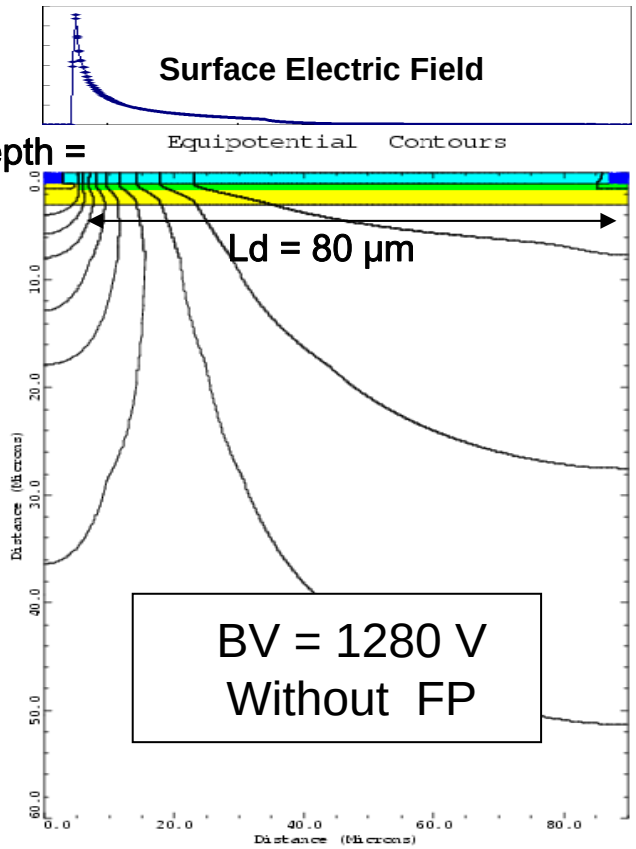
- REduced SURface Field
- Breakdown in the bulk
- Thick and lightly doped p-layer

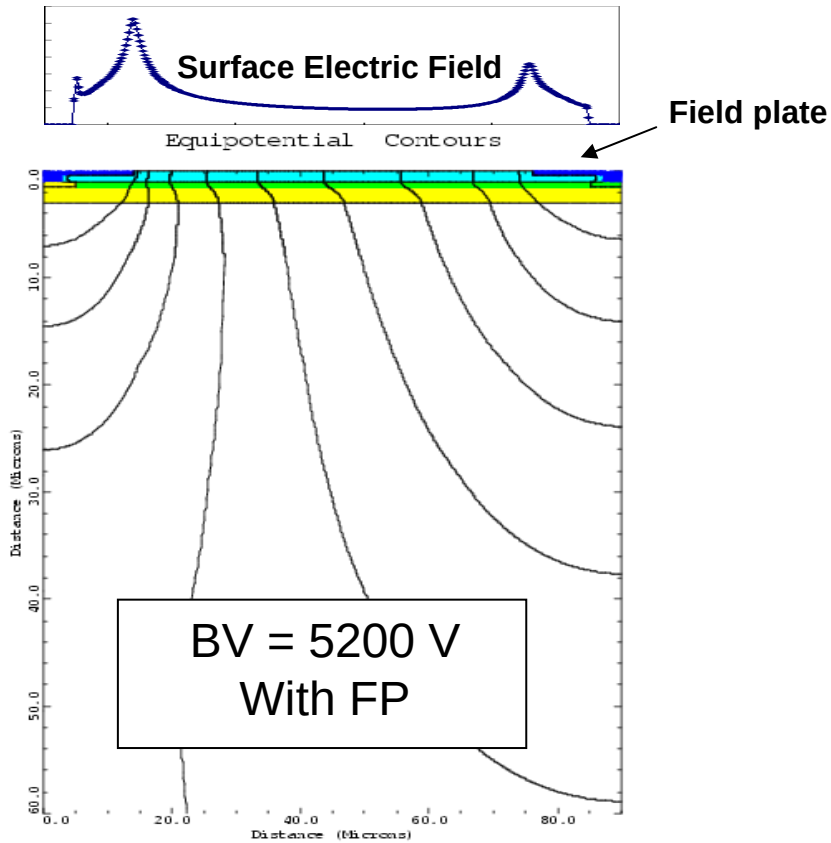


- Semi-insulating substrate
- Charge compensation of n- and p-type epi-layers

Effects of Field Plates on Proposed Structure

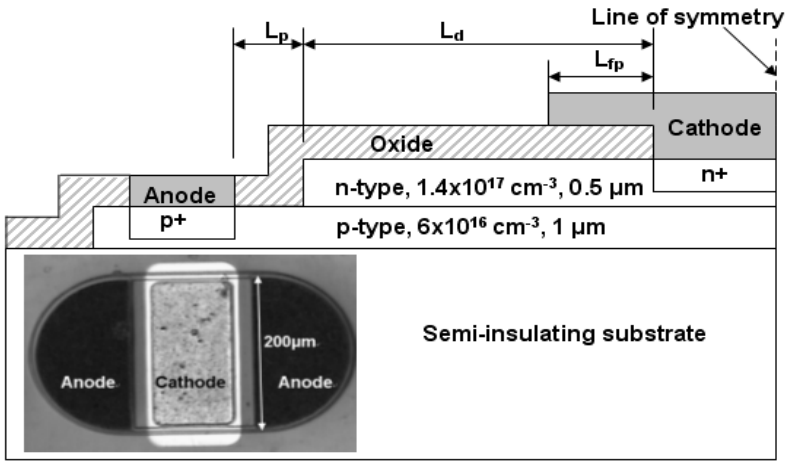
Junction depth = 0.5 μm



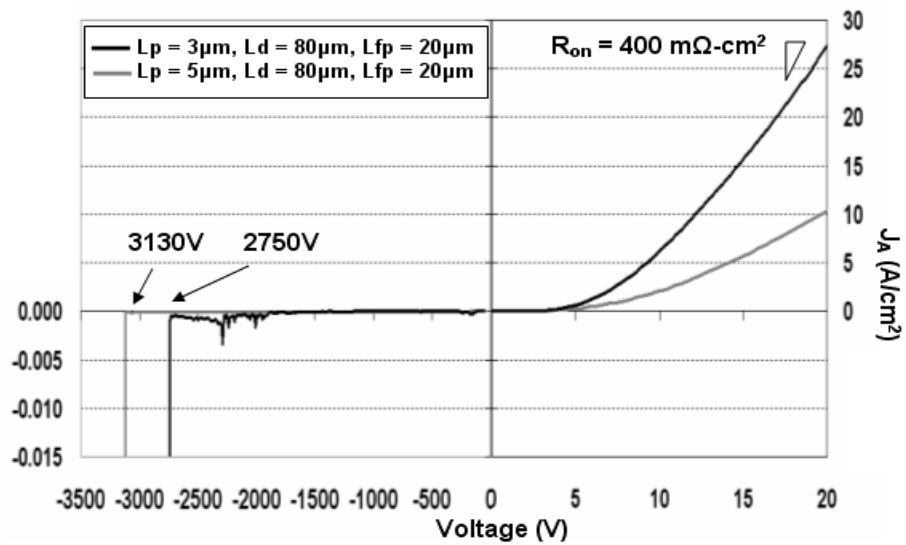


- Field plates reduce electric field crowding at the junction corners.

High Voltage Lateral SiC Diodes



Schematic cross-section of the lateral diode

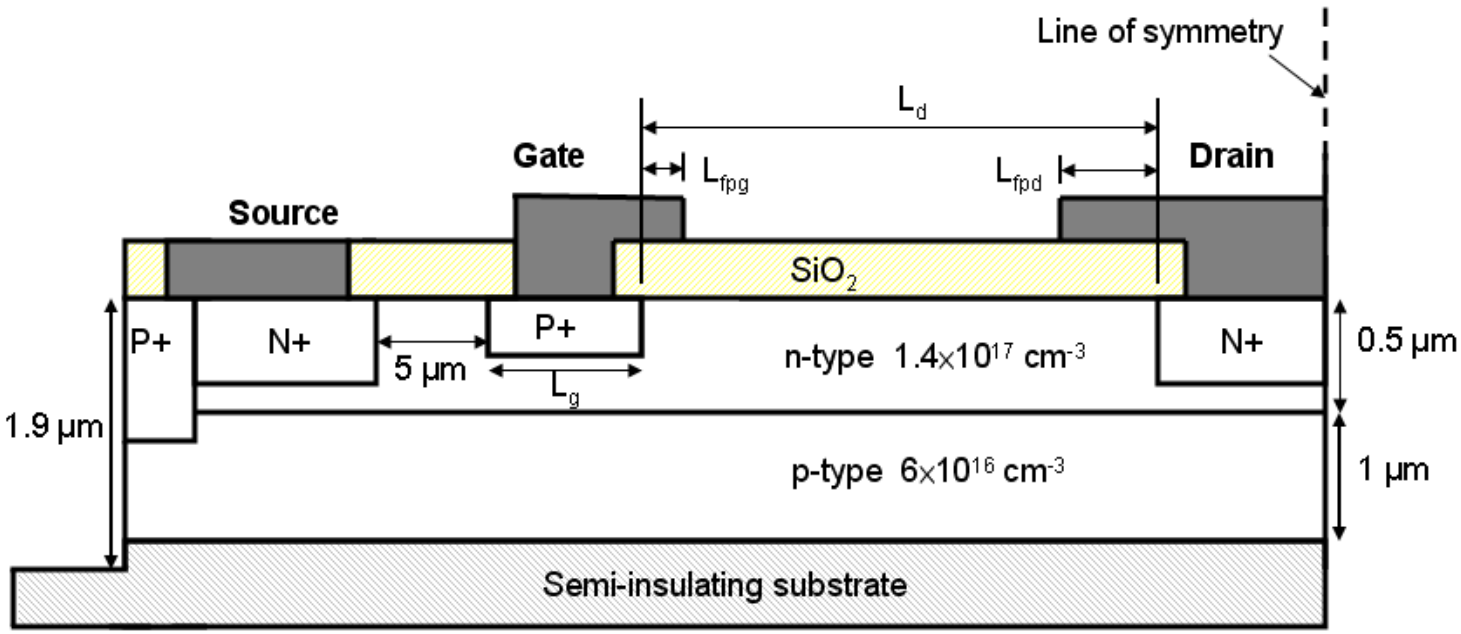


Forward and reverse IVs

- BV = 3130 V has been demonstrated on a Ld = 80 µm lateral diode.

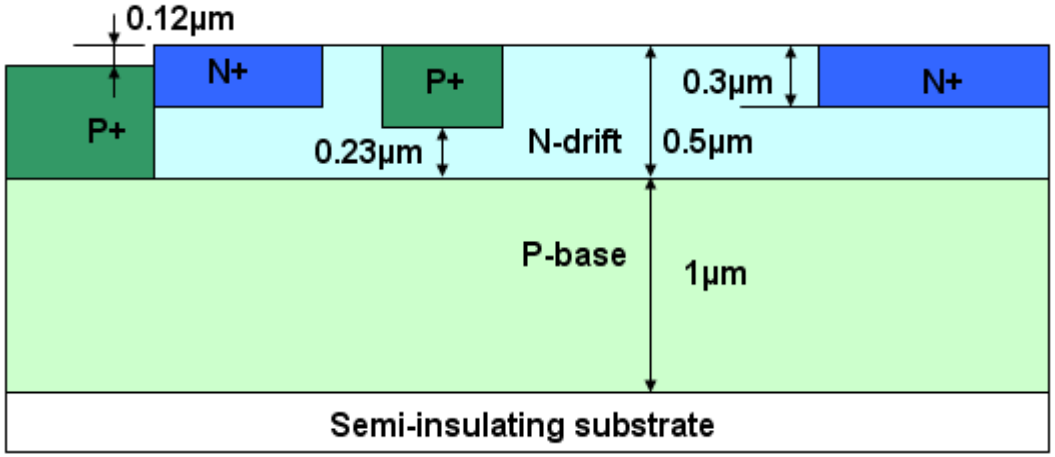
C. –F. Huang et al., *IEEE Electron Device Letters,* **29**, 83-85 (2008)

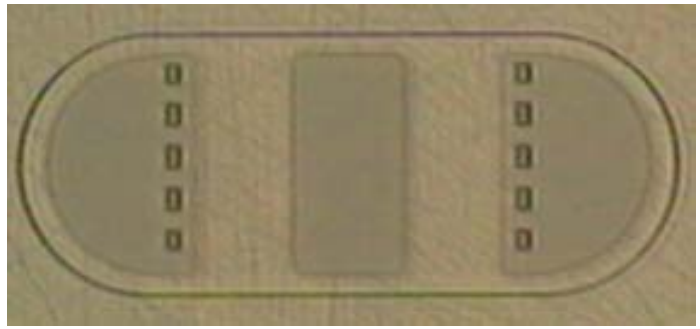
4H-SiC Lateral JFET Design



- $Q_n = 7E12\ cm^{-2} < Q_c = 1.1E13\ cm^{-2}$
- $Q_p = 6E12\ cm^{-2} < Q_c$
- $L_d = 25, 50, 80, 100\ \mu m$
- $L_g = 9, 15\ \mu m$

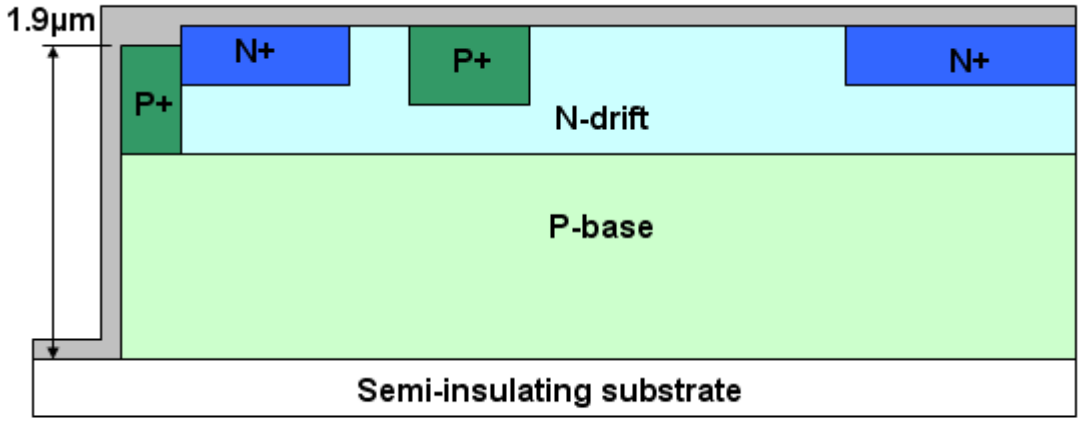
Fabrication of 4H-SiC Lateral JFETs (1)

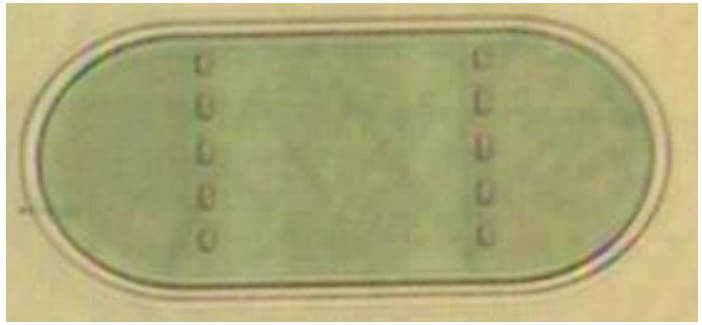




- 0.12 μm RIE for P+ sinker
- Aluminum implantation at 650 ^{o}C for P+ gate and P+ sinker
- Nitrogen implantation at room temperature for source and drain
- Implant activation at 1650 ^{o}C for 30 min in Ar

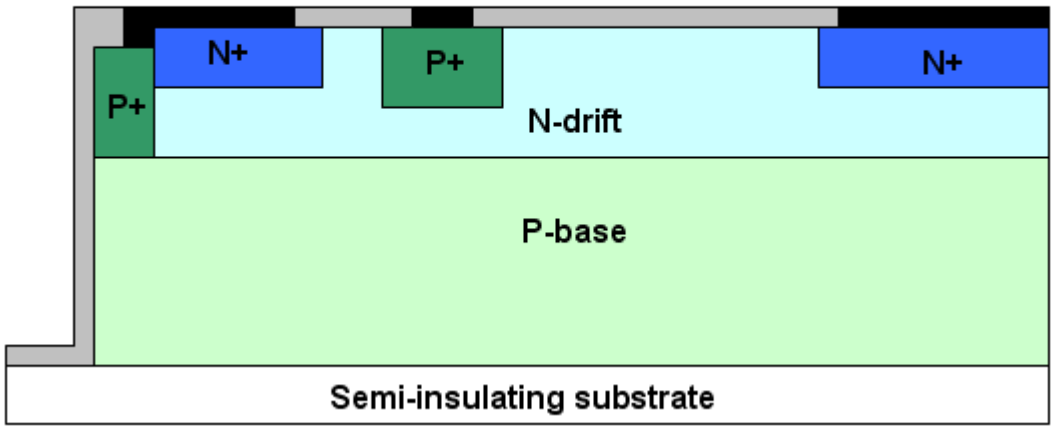
Fabrication of 4H-SiC Lateral JFETs (2)

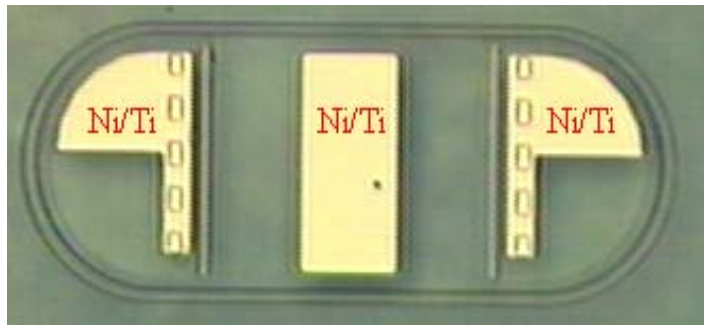




- RIE 1.9 μm in SF_6/O_2 to form isolation trenches
- Thermal oxidation at 1180 ^oC for 6 hrs to passivate the surface

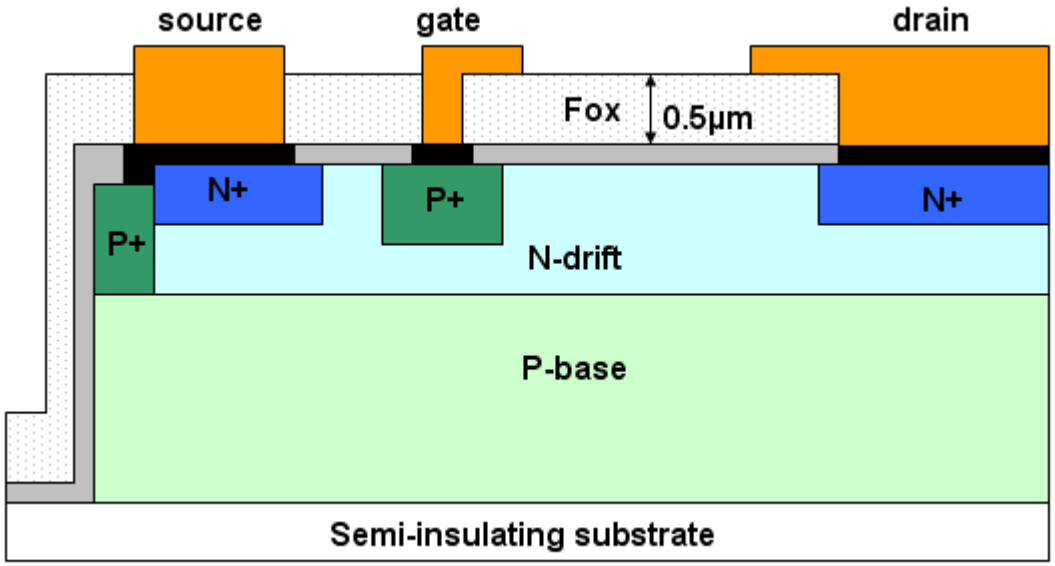
Fabrication of 4H-SiC Lateral JFETs (3)

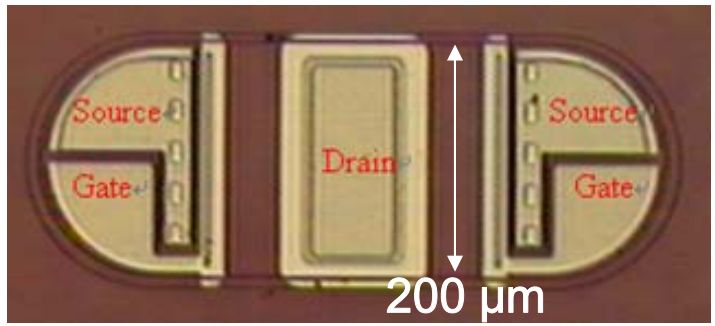




- Lateral out-diffusion of Al was observed during high temperature anneal in a test run
- E-beam evaporate Ti/Ni as both n- and p-type contact metals
- Anneal both contacts at 1100 ^{o}C for 3 mins in vacuum

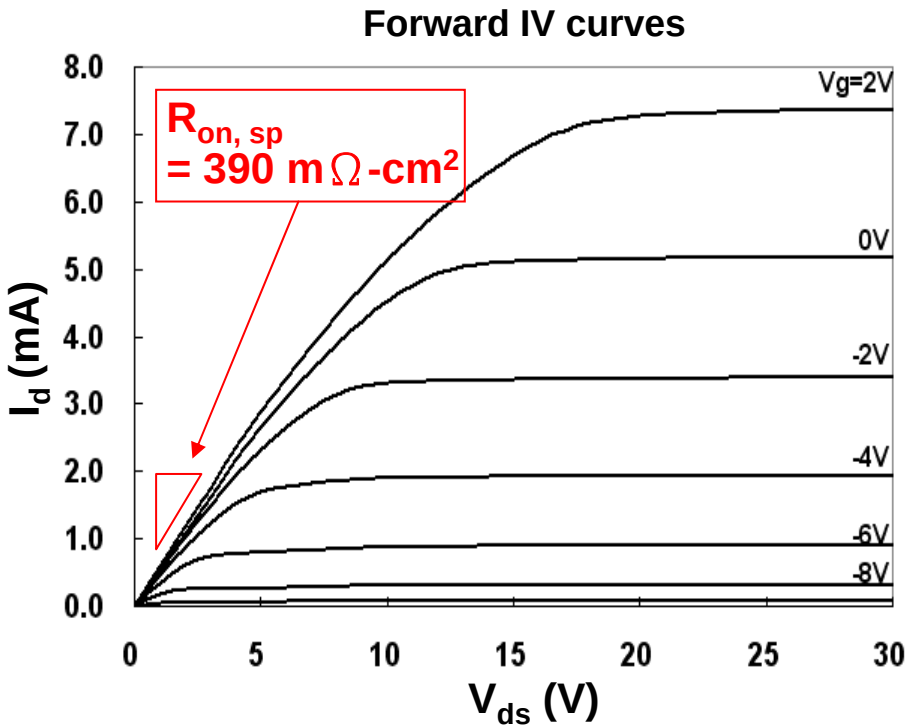
Fabrication of 4H-SiC Lateral JFETs (4)

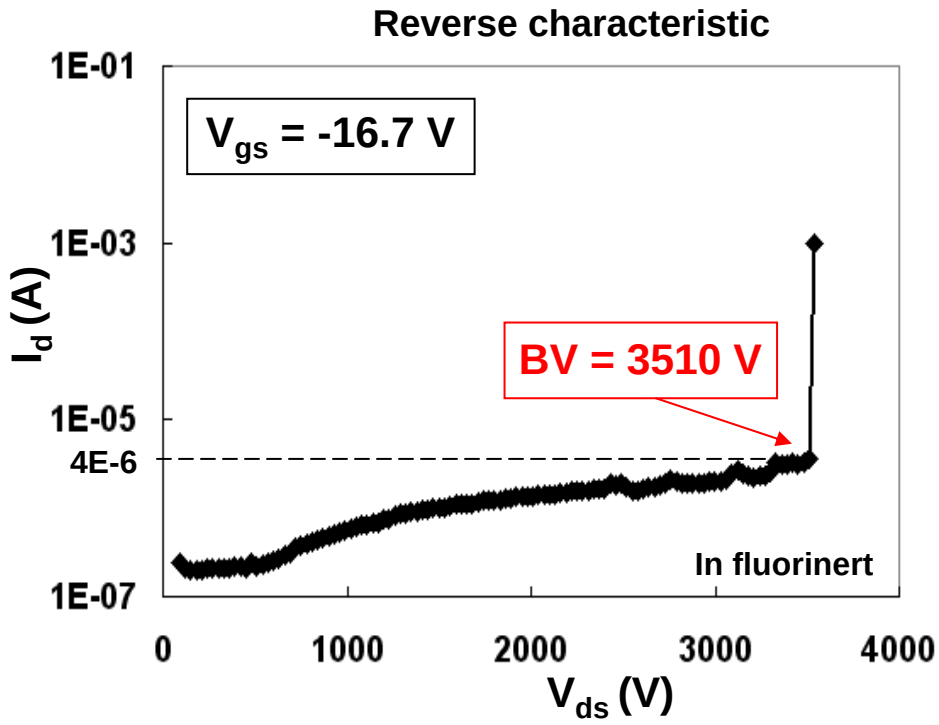




- Deposit 0.5 μm of PECVD oxide as field oxide
- Open windows
- E-beam evaporate 0.8 μm of Al/Ti as pads and field plates

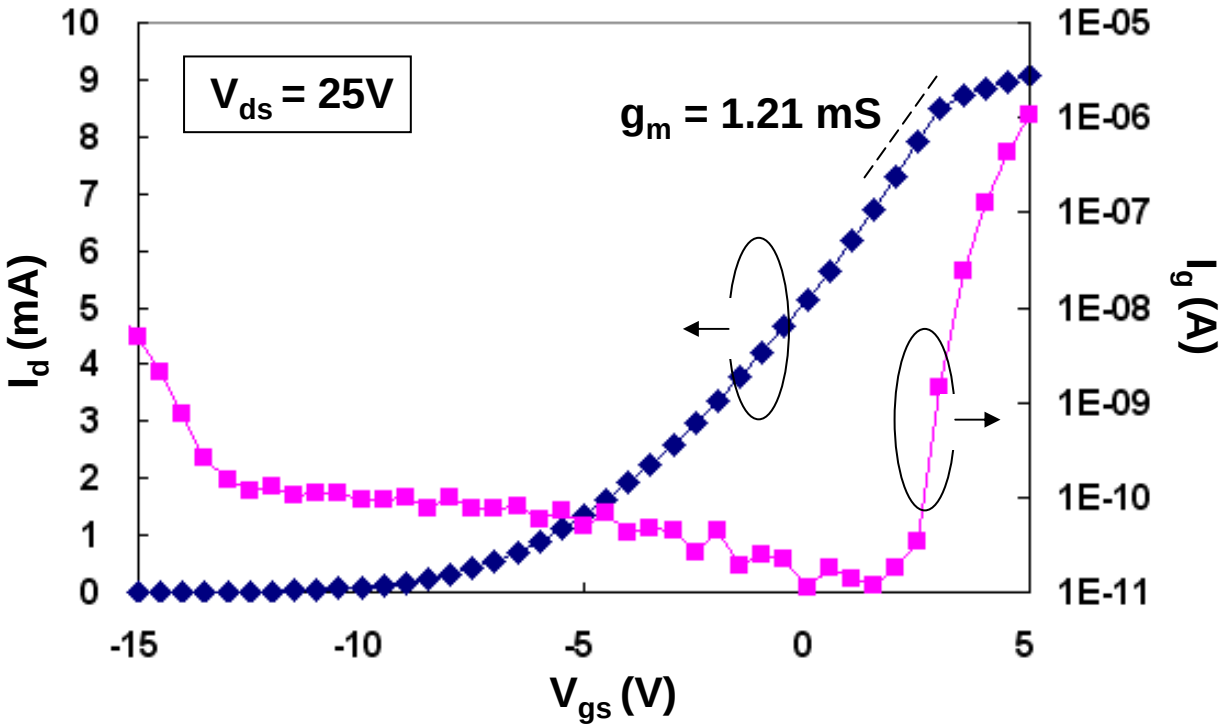
Forward and Reverse Characteristics





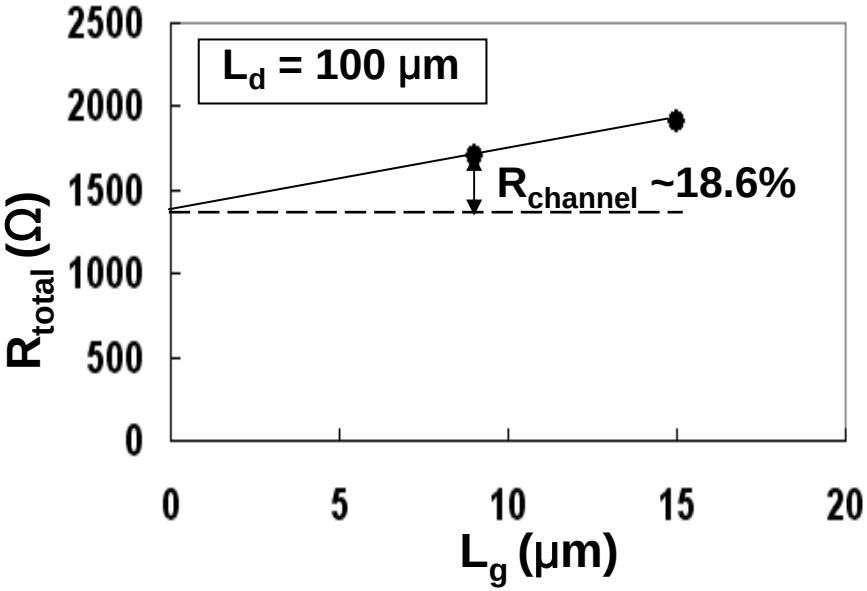
- BV = 3510 V and $R_{on,sp}$ = 390 mΩ-cm² were achieved on a L_g = 9 μm, L_d = 100 μm device. (L_{fpg} = 10 μm, L_{fpd} = 25 μm)
- The active area is 0.0228 mm².
- I_{on}/I_{off} > 1000

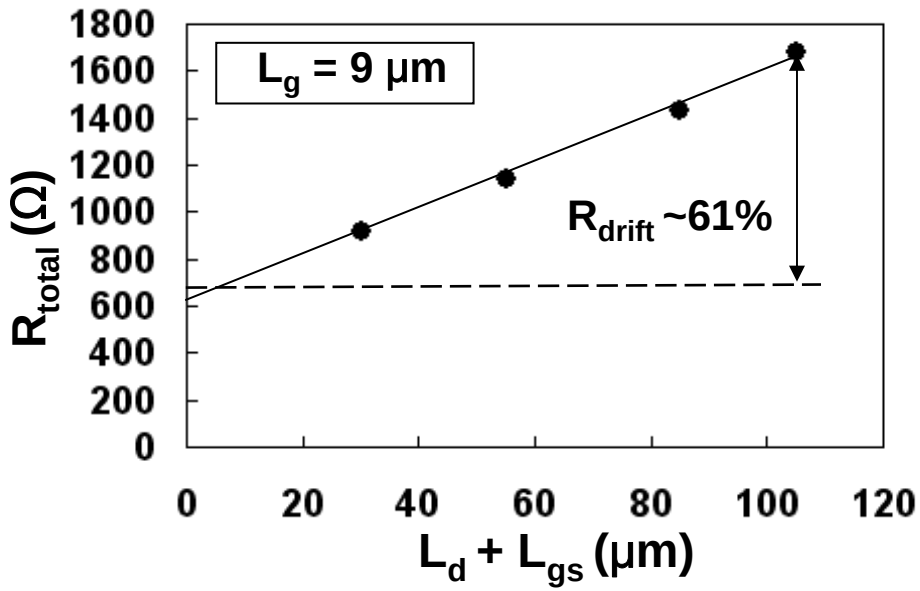
Transfer Characteristics



- I_g < 1E-8 A until gate junction turns on at V_{gs} = 3 V.
- The pinch-off voltage is about -11 V. Peak g_m is 1.21 mS at V_{gs} = 2.5 V.

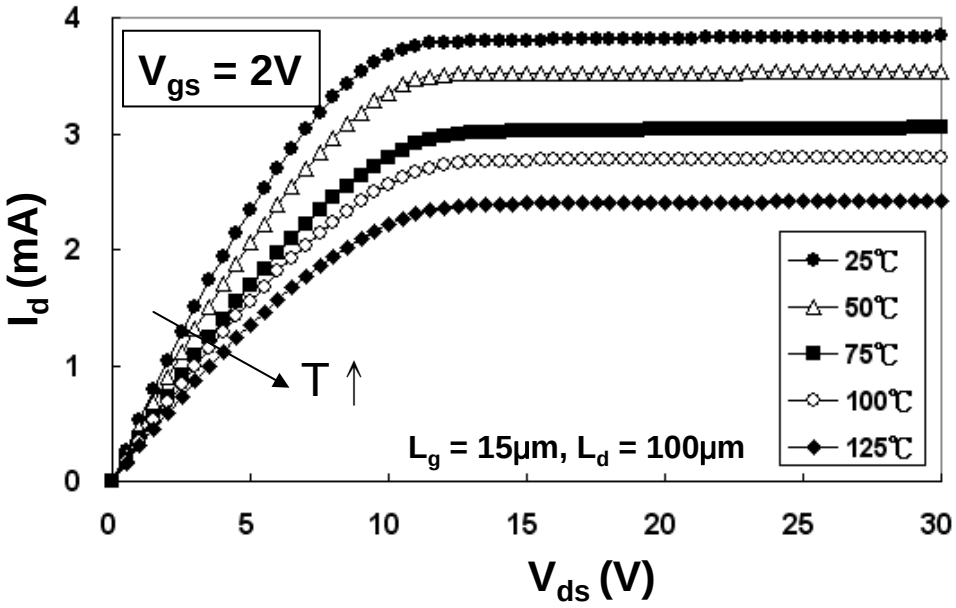
R_{drift} and $R_{channel}$

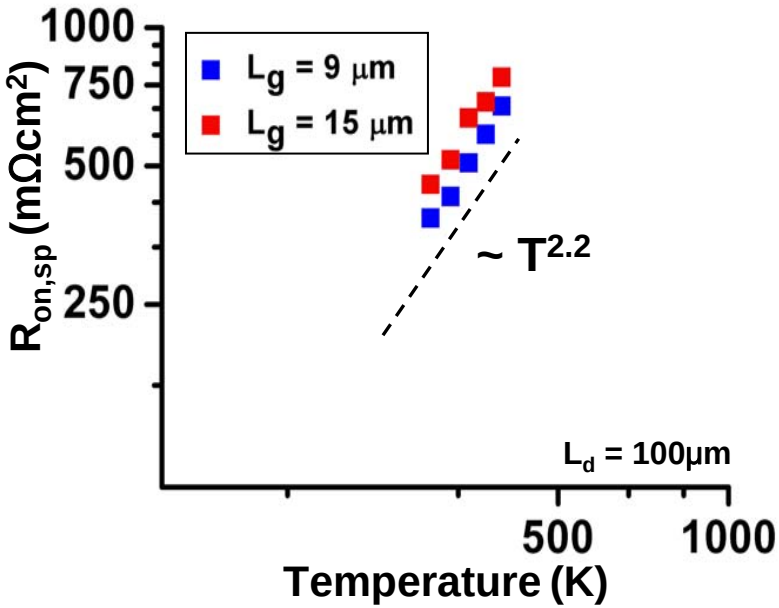




- In a Lg = 9 μm, Ld = 100 μm device, R_{drift} is about 61% of R_{total} and R_{ch} is about 18.6%.

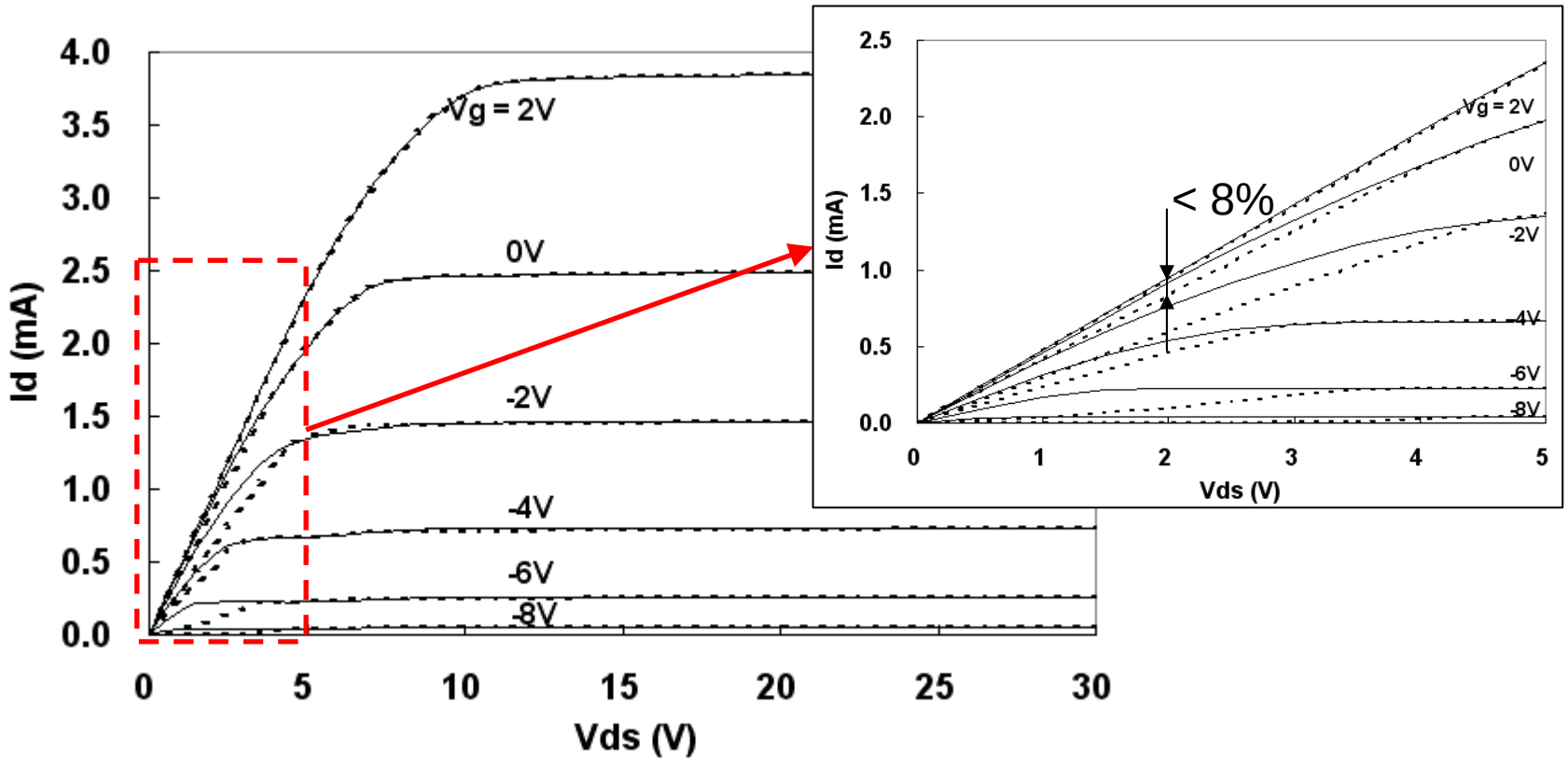
Temperature Characterization





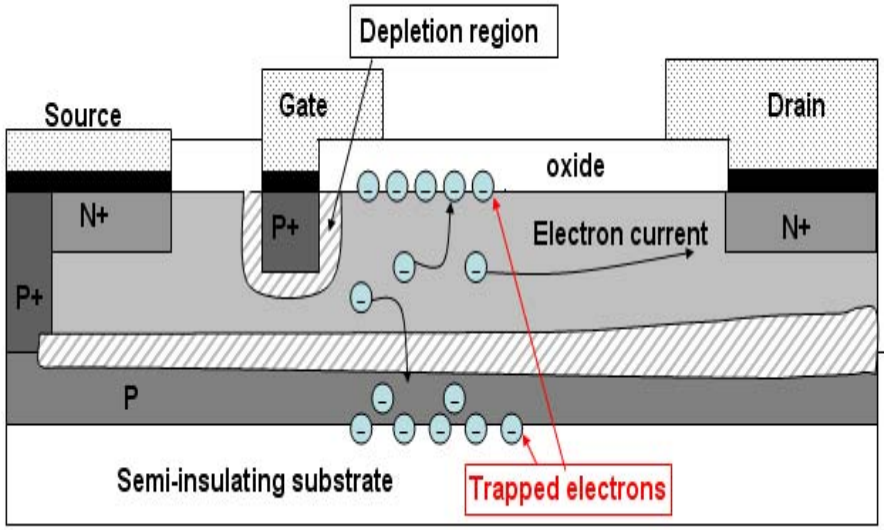
- $R_{on,sp}$ increases with temperature following a $T^{2.2}$ relationship ($\mu_n \sim T^{-2.4}$ in 4H-SiC).

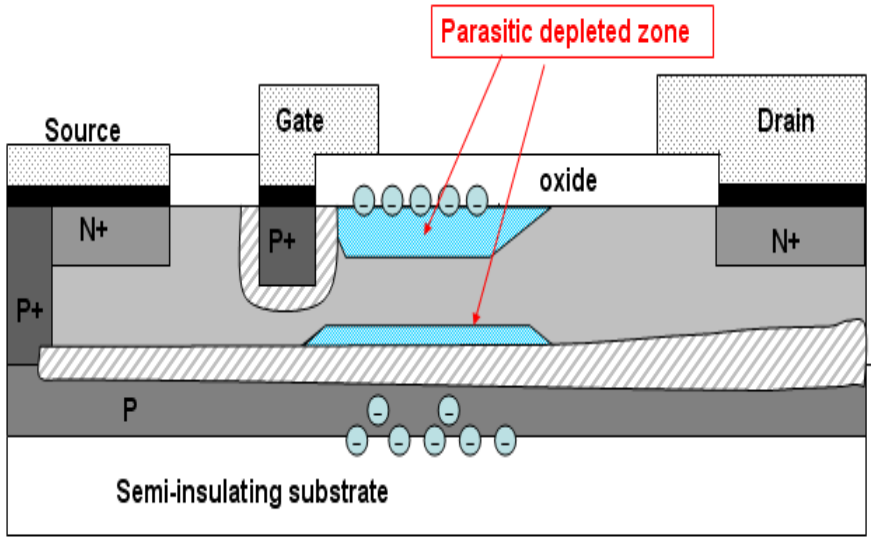
Drain Current Drift



- Drain current drift is observed as in 4H-SiC MESFETs.
- The reduction of drain current is less than 8% at V_{gs} = 0 V.

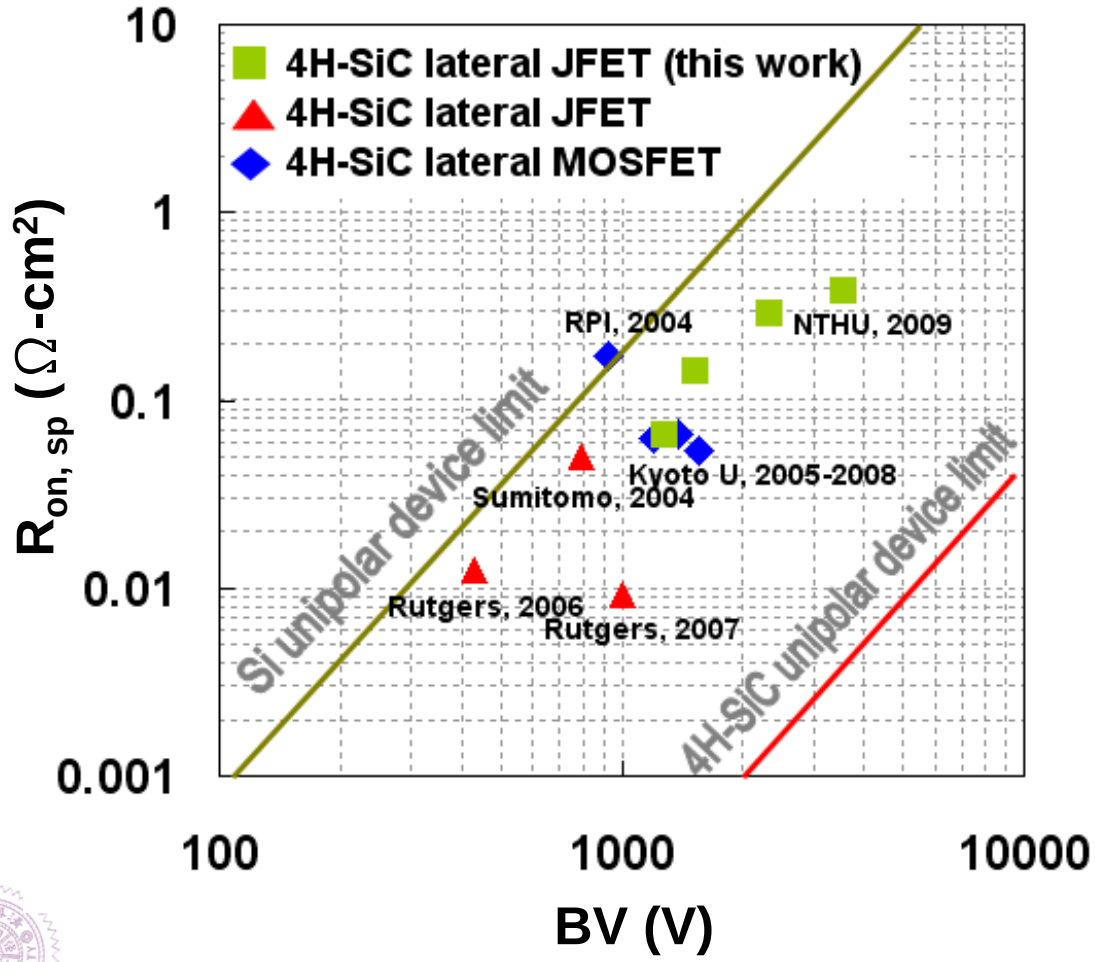
Trapping Effects





- The trapped electrons deplete the channel and the n-type layer.
- The trapped electron density is less than 8% of Q_n. Its effects on charge balance and BV are not clear at this point.

Comparison of 4H-SiC Lateral Devices



L_d (μm)	BV (kV)	$R_{on,sp}$ (mΩ-cm^2)
25	1.27	66
50	1.51	145
80	2.32	291
100	3.51	390

BV^2/R_{on} = 32 MW/cm^2

C. F. Huang DRC 2009

Summary

- High voltage SiC lateral JFETs are demonstrated on a semi-insulating substrate.
- $R_{on,sp}$ = 390 mΩ-cm^2, BV = 3510 V for a Lg = 9 μm, Ld = 100 μm device.
- R_{drift} contributes about 61 % of R_{total} in a Lg = 9 μm, Ld = 100 μm device. $R_{channel}$ contributes about 18.6 %.
- Drain current drift was observed and attributed to trapping effects.