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Fully Analytical Modeling of Cu Interconnects up to 110 GHz

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Copper interconnects with and without the grounded shielding on the silicon substrate are modeled from 1 to 110 GHz. The fully-analytical model is composed of the cascaded lumped resistor–inductor–conductor–capacitor (RLGC) circuit elements with 20 sections, and featured physical-based, scalable, and frequency-dependent characteristics. An excellent agreement is obtained between the measured, simulated, and modeled *S*-parameters without any optimization procedure. The proposed approach can be applied for interconnect modeling for integrated-circuits over a wide frequency range.
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KEYWORDS: copper, interconnects, silicon substrate, model, RLGC, *S*-parameters, integrated circuits

1. Introduction

The increased date rates have pushed the operation frequency of the integrated circuits using advanced complementary metal–oxide–semiconductor (CMOS) technologies up to 100 GHz.[1,2] The interconnects made of copper play an important role in these circuits since their impact on circuit characteristics can no longer be neglected. Various interconnects modeling approaches have been reported.[3–6] An analytical approach has been used by considering only part of the high-frequency effects, and was verified up to relative low frequencies.[3] In addition, several semi-analytical interconnect models were developed for a better agreement with the simulated[4] or the measured results.[5,6] In this study, a simple approach with multi-section resistor–inductor–conductor–capacitor (RLGC) elements, but fully physical-based and scalable, is proposed and verified up to 110 GHz. With the lumped RLGC equivalent circuit, the components in the model take into account all of the important high-frequency effects, such as the substrate skin effect[7,8] and the proximity effect[9] for the frequency-dependent inductances and resistances. Each component relates directly to the physical structure of the interconnect resulting in a fully-scalable model over a wide frequency range without any optimization procedure.

Additionally, the Cu interconnects with and without grounded shielding for the silicon (Si) substrate are both studied. Compared with the shielded case, unshielded interconnect model needs to consider the effects introduced by the lossy Si substrate. Both types of interconnects find their applications in circuits. For example, the shielded interconnects are often adopted in microwave circuits to minimize the signal loss. On the other hand, the unshielded interconnects are commonly used in high-speed very-large-scale integration (VLSI) circuits to save the chip area, where the associated ground plane may not be close to the signal line. The results demonstrate that a simple multi-section RLGC model can be used for both types of interconnects by carefully considering the high frequency effects of each component.

2. Modeling of Interconnects

The Cu interconnects are fabricated using a standard 0.13-μm CMOS process which provides eight metal layers for flexible interconnect design. The interconnects with and without the grounded Si-substrate shielding in this study are both depicted in Figs. 1(a) and 1(b), respectively. The signal line is realized by metal eight (M8), with a width and a thickness of 2.5 μm (w_s) and 3.3 μm (t_s), respectively, and the descriptions for all the employed geometrical and physical parameters are summarized in Table I. The grounded Si substrate shielding is realized by M1 with a thickness of 0.28 μm (t_g). A silicon dioxide (SiO_2) layer with a thickness of 6.3 μm (t_{ox}) and a ε_r' of 4.04 are used between M8 and M1, while that with a thickness of 7.07 μm (t_{ox1}) and a ε_r' of 4.05 are employed between M8 and the Si substrate for the case without the substrate shielding.

Modeling of the Cu interconnects is based on the distributed RLGC circuit model with n sections due to the advantages of a simple yet physical-based circuit topology, as shown in Fig. 2. The section number n can be calculated by the following equation,[10] which is based on the assumption that a line can be modeled sufficiently by a section of lumped RLGC components if the length is smaller than or equal to one tenth of the wavelength:

$$n = 10 \times \frac{f_m \times l}{v}, \tag{1}$$

where f_m is the maximum operation frequency, l is the length of the line, and v is the wave velocity. In addition, it was found that the interconnect with a length of 1000 μm can be modeled precisely by only 20 RLGC sections. The calculation of each component in the lumped interconnect model for both with (denoted as R_{w_s}, L_{w_s}, G_{w_s}, and C_{w_s}) and without (denoted as R_{wo_s}, L_{wo_s}, G_{wo_s}, and C_{wo_s}) substrate shielding are described as follows.

2.1 *Cu interconnects with substrate shielding*

In this case, the RLGC components only relate to the top and bottom metals and the SiO_2 layers since the Si substrate has been isolated by the ground plane. The resistance R_{w_s} is the sum of the DC and AC resistances for both signal and ground lines. The skin effect dominates the AC resistance, which can be modeled precisely by considering the finite metal width and thickness.[3] The resistance R_{w_s} can be calculated as:

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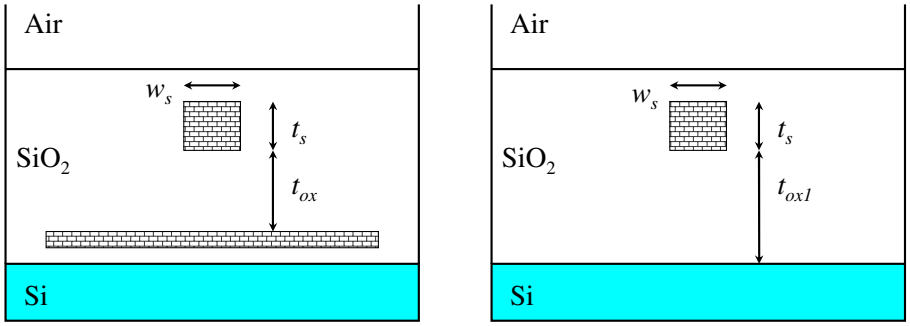

Fig. 1. (Color online) Cross-sections of the Cu interconnects (a) with and (b) without and grounded Si-substrate shielding.

Table I. Description for geometrical and physical parameters of the interconnects.

Symbol	Description
w_s, w_g	Metal width of signal and ground lines
t_s, t_g	Metal thickness of signal and ground lines
t_{ox}	Distance between signal and ground layers
t_{ox1}	Distance between signal layer and Si substrate
σ_s, σ_g	Metal Conductivity of signal and ground line
σ_{Si}	Conductivity of Si substrate
ε_r', ε_r''	Real and imaginary part of relative dielectric constant
ε_0, μ_0	Permittivity and permeability of free space
δ_s, δ_g	Skin depth of signal and ground line
δ_{si}	Skin depth of Si substrate

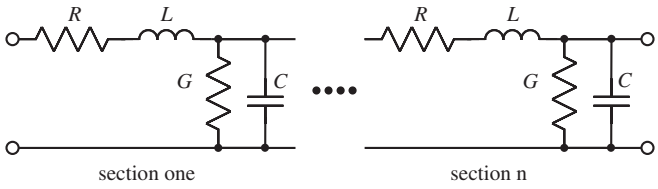

Fig. 2. The lumped RLGC circuit model with n sections.

$$R_{w\_s} = \frac{1}{\sigma_s w_s t_s} + R_{AC\_s} + \frac{1}{\sigma_g w_g t_g} + R_{AC\_g}, \tag{2}$$

where

$$R_{AC\_s} = \frac{1}{\sigma_s w_s} \frac{1}{\delta_s[1 - \exp(-t_s/\delta_s)](1 + t_s/w_s)}, \tag{3}$$

$$R_{AC\_g} = \frac{1}{\sigma_g w_g} \frac{1}{\delta_g[1 - \exp(-t_g/\delta_g)](1 + t_g/w_g)}, \tag{4}$$

where R_{AC_s} and R_{AC_g} are the AC resistances of the signal and ground lines, respectively. The inductance L_{w_s} is mainly determined by the current loop area. Within the SiO_2 layer, the loop area is frequency independent leading to an external inductance L_{ext}, which can be obtained by the geometric mean distance (g.m.d.) for finite metal width and thickness.[11] In addition, since the current loop area inside the metal is affected by both skin and proximity effects, a frequency-dependent internal inductance L_{int} should be considered.[9] Consequently, the total inductance L_{w_s} is a sum of L_{ext} and L_{int} as shown below:

$$L_{int} = \frac{\mu_0}{2\pi} \frac{3}{8} \tanh\left(\frac{2\pi\delta_s}{w_s + t_s}\right), \tag{5}$$

$$L_{ext} = (\mu_0/2\pi)(2\ln[R_{12}] - \ln[r_1] - \ln[r_2]), \tag{6}$$

where

$$\ln[R_{12}] = \ln\left[100\left(\frac{2t_{ox} + t_s + t_g}{2}\right)\right] + k_1, \tag{7}$$

$$r_1 = 100 \times e^{-3/2}(w_s + t_s), \tag{8}$$

$$r_2 = 100 \times e^{-3/2}(w_g + t_g), \tag{9}$$

and where R_{12} is the g.m.d. between the signal and ground lines, k_1 is a geometry dependent factor, and r_1 and r_2 represent the g.m.d. of the signal and ground lines, respectively.

Since the loss of the SiO_2 layer needs to be considered, a complex dielectric constant is employed for the conductance calculation. The conductance G_{w_s} is estimated by a parallel-plate structure, and can be represented as:

$$G_{w\_s} = \varepsilon_0 \varepsilon_r'' \omega \frac{w_s}{t_{ox}}, \tag{10}$$

where ω is angular frequency. A conductance increased proportional to the operation frequency can be expected. In the modeled frequency range, this parameter is negligible for a low-loss dielectric SiO_2 in a typical CMOS process.

For the modeled line structure, the electric field distributes in both the air and the SiO_2 layers, which results in a geometry-dependent ε_r'.[3] In addition, a fringing capacitance is taken into account for the sidewalls of the signal line, which can introduce a significant parasitic capacitance.[12] The capacitance C_{w_s} includes both the parallel-plate and the fringing capacitances, and can be written as:

$$C_{w\_s} = \varepsilon_0 \varepsilon_{reff} \frac{w_s}{t_{ox}} + \varepsilon_0 \varepsilon_{reff} \frac{2\pi}{A_f}, \tag{11}$$

where

$$\varepsilon_{reff} = \frac{\varepsilon_r' + 1}{2} + \frac{\varepsilon_r' - 1}{2(\sqrt{(1 + 10t_{ox}/w_s)})}, \tag{12}$$

$$A_f = \ln\left(1 + \frac{2t_{ox}}{t_s} + \sqrt{\frac{2t_{ox}}{t_s}\left(\frac{2t_{ox}}{t_s} + 2\right)}\right). \tag{13}$$

The dispersion effect of ε_r' was not considered due to the wavelength is significantly larger than the width w_s and thickness t_s of the signal line.

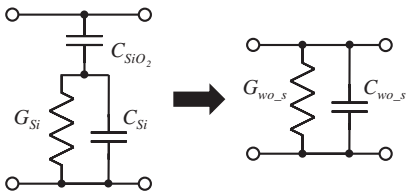

Fig. 3. Equivalent circuit model for the Si substrate and the SiO_2 layer.

2.2 *Cu interconnects without substrate shielding*

For the Cu interconnects without substrate shielding, the electromagnetic wave can penetrate into the lossy Si substrate, which is referred as the substrate skin effect.[7,8] As a result, the series impedance (Z_{Si}) of the interconnects can be calculated as:

$$Z_{Si} = \frac{1}{\sigma_s w_s t_s} + j\omega \frac{\mu_0}{2\pi} \ln\left[\frac{2t_{eq} + \delta_{Si} - j\delta_{Si}}{r_{eq}}\right], \quad (14)$$

where

$$t_{eq} = t_{ox1} + (t_s - w_s)/4, \quad (15)$$

$$r_{eq} = (t_s + w_s)/4. \quad (16)$$

In this case, R_{wo_s} can be obtained from the real part of Z_{Si}, and L_{wo_s} is the imaginary part of Z_{Si} divided by ω. As can be seen, R_{wo_s} is determined not only by the metal signal line but also by the Si substrate. In addition, as a function of δ_{Si}, L_{wo_s} presents a frequency-dependent characteristic.

Based on the physical structure, the substrate underneath the signal line can be modeled by a Si conductance (G_{Si}) and a Si capacitance (C_{Si}) first connected in parallel, and then in series with a SiO_2 capacitance (C_{SiO_2}), as shown in Fig. 3. The model can then be further simplified to a parallel GC network of G_{wo_s} and C_{wo_s}, and can be written as:

$$G_{wo\_s} = \mathrm{Re}\left[1 \Big/ \left(\frac{1}{G_{Si} + sC_{Si}} + \frac{1}{sC_{SiO_2}}\right)\right], \quad (17)$$

$$C_{wo\_s} = \mathrm{Im}\left[1 \Big/ \left(\frac{1}{G_{Si} + sC_{Si}} + \frac{1}{sC_{SiO_2}}\right)\right] \Big/ \omega, \quad (18)$$

These three parameters (G_{Si}, C_{Si}, and C_{SiO_2}) are obtained based on the physical structure, and considered the geometry-dependent effective dielectric constants in a parallel plate structure similar to eqs. (10)–(13).

3. Results and Discussion

Based on the equations described above, the modeled frequency responses of the Cu interconnects are obtained from the software Agilent Advanced Design System (ADS).[13] For comparison, the simulation are also performed by using the industry standard full-wave electromagnetic (EM) simulator SONNET.[14] The measured results are obtained from the two test structures. The Cu interconnects were measured on-wafer with coplanar ground–signal–ground (GSG) probes from 1 to 110 GHz. The deembedding procedure was done by using two interconnects of 1200 and 200 μm to obtain the *S*-parameters of a 1000 μm line.[15,16] Figures 4 and 5 show the measured, simulated, and modeled results for the interconnects with and without the Si-substrate shielding, respectively. For both types of Cu interconnects, as can be seen, the modeled *S*-parameters are

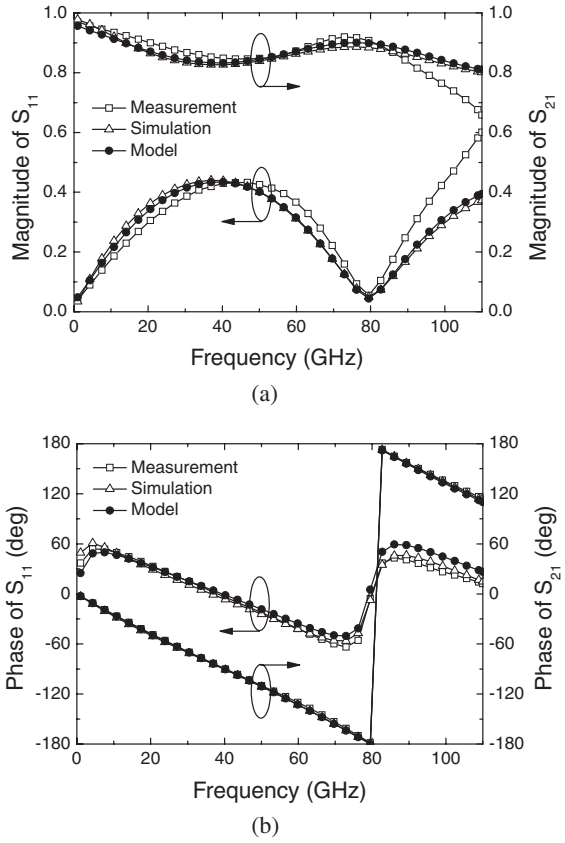

Fig. 4. (a) Magnitude and (b) phase of the measured, simulated, and modeled *S*-parameters of the Cu interconnects with the Si-substrate shielding. The length of the line is 1000 μm and *n* is 20.

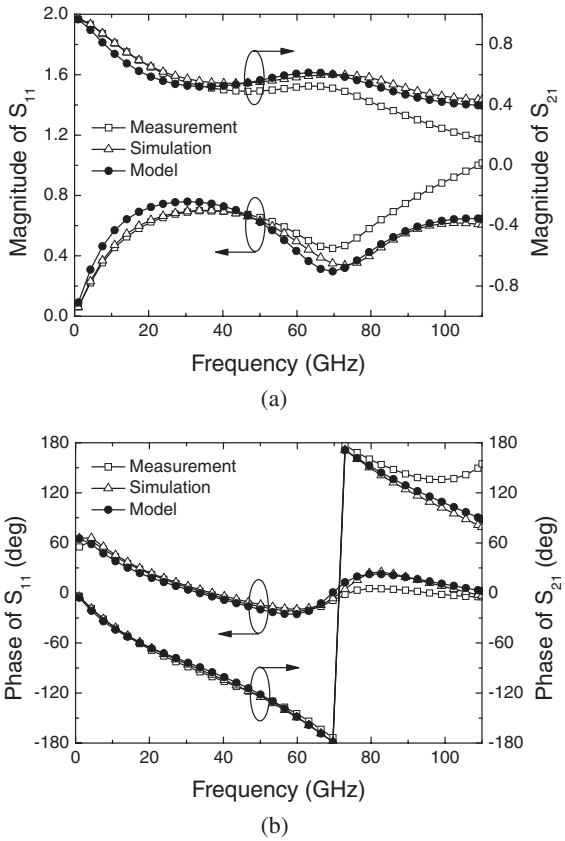

Fig. 5. (a) Magnitude and (b) phase of the measured, simulated, and modeled *S*-parameters of the Cu interconnects without the Si-substrate shielding. The length of the line is 1000 μm and *n* is 20.

in excellent agreement with the simulated and measured results in a wide frequency range. The increased discrepancy observed between the measured and modeled results at high frequencies may result from the deembedding inaccuracy of the symmetrical pad assumption.[17] For the interconnects without the Si-substrate shielding, the signal loss is large and the phase of S_{21} is not linear due to the effect from the lossy Si substrate. On the other hand, the interconnects with the Si-substrate shielding is more suitable for high-frequency and wideband applications, where low loss and low phase distortion is the major concerns.

4. Conclusions

A fully analytical approach with scalability for the Cu interconnects in a standard 0.13-μm CMOS process was developed and verified up to 110 GHz. By carefully considering the frequency-dependent effects of each RLGC component, excellent agreement was observed between measured, modeled, and simulated *S*-parameters. The proposed simple approach not only provided the physical insight but also showed excellent modeling accuracy for both shielded- and unshielded-type interconnects over a wide frequency range without any optimization procedure.

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