Impact of STI Effect on Flicker Noise in 0.13-μm RF nMOSFETs

Chih-Yuan Chan, Yu-Syuan Lin, Yen-Chun Huang, Shawn S. H. Hsu, *Member, IEEE*, and Ying-Zong Juang

***Abstract*—This paper reports on the impact of shallow-trench isolation (STI) on flicker noise characteristics in 0.13-μm RF nMOSFETs. The drain noise current spectral density was measured in both triode and saturation regions for a more complete study. The devices with a relatively small finger width and a large finger number ($W = 1$ μm/$N_{\rm finger} = 40$ and $W = 5$ μm/$N_{\rm finger} = 8$) presented more pronounced generation–recombination (G–R) noise characteristics compared to those with $W = 10$ μm/$N_{\rm finger} = 4$. In addition, a wide noise level variation of more than one order of magnitude was associated with the more obvious G–R noise components. The observed trends can be explained by the nonuniform stress effect of STI and also the associated traps at the edge of the gate finger between STI and the active region. To further study the noise mechanism, the single-finger devices with different STI-to-gate distances [SA(SB) = 0.6, 1.2, and 10 μm] were investigated. The measured results provided a direct evidence of STI effect on flicker noise characteristics. The activation energy of the traps was extracted at various temperatures in a range from $E_C - 0.397$ to $E_C - 0.54$ eV. Moreover, the calculated standard deviation $\sigma_{\rm dB}$ showed a strong dependence of noise variation on device geometry ($\sigma_{\rm dB} = 2.95$ dB for $W = 1$ μm/$N_{\rm finger} = 40$ and $\sigma_{\rm dB} = 1.54$ dB for $W = 10$ μm/$N_{\rm finger} = 4$). The analysis suggests that the carrier number fluctuation model with the correlated mobility scattering is more suitable for the noise characteristics in these devices.**

***Index Terms*—Low-frequency noise, MOSFETs, shallow-trench isolation (STI), stress.**

I. Introduction

THE IMPACT of STI on MOSFET characteristics has been studied, and the distance between the edge of shallow-trench isolation (STI) to the gate has been demonstrated to play an important role in device dc characteristics [1]–[3]. The mechanical stress introduced by STI and stress-control layers on flicker noise in CMOS has also been studied previously [4], [5]. The traps/interface states are a major flicker noise origin in MOS devices, which can be a crucial factor in the performance of nonlinear radio frequency integrated circuits such as voltage-controlled oscillators (VCOs) and mixers [6]. In many mixed-mode circuits, flicker noise also degrades the signal-to-noise ratio. Studies focused on flicker noise modeling for CMOS technologies have also been published [7], [8]. However, little has been reported regarding the impact of STI-induced stress and traps on flicker noise [9]. Neither a detailed study on the physical origins nor on the generation–recombination (G–R) noise of devices was discussed. In addition, the effect of device geometry on G–R noise was not investigated systematically.

In this paper, the flicker noise characteristics of 0.13-μm RF nMOSFETs with a fixed total device width but various finger widths and finger numbers are investigated. Many devices of each type from different chips are characterized to obtain a statistical conclusion. The devices with a single finger but various STI distances are also measured to further identify the noise mechanisms. We found that the flicker noise characteristics regarding the variation from different chips and the corresponding G–R components are a strong function of the RF device geometry even with the same W $\times$ L values due to the STI effect. In addition, the noise level variation is modeled quantitatively [10]–[12]. The conclusion provides recommendation about device design and selection for a smaller flicker noise deviation and a lower noise level. The STI effect on flicker noise can be foreseen to be more pronounced when technology keeps scaling down to a smaller feature size.

This paper is organized as follows. Section II describes the noise measurement setup and the layout of the devices. Section III presents the experimental results and discussion, which includes the dc and flicker noise characteristics, the extraction of the trap activation energy, and the noise variation modeling. Section IV concludes this work.

II. Flicker Noise Measurement Setup and Device Structures

Fig. 1(a) shows the flicker noise measurement setup, where the low-noise preamplifier with a low noise floor is critical in the system. The noise voltage converted from the device drain noise current by the load resistor R_L is detected by the dynamic signal analyzer. Low-loss RF cables and probes with excellent ground shielding were used for the signal paths. In addition, the devices and the system including the preamplifier and the probe station were enclosed in a shielding box to further reduce the environmental interference. Moreover, a battery-powered dc voltage source was employed to prevent the additional noise introduced by the power supply. The noise measurements were performed in a range of 10 Hz to 100 kHz, and the noise floor of the system was well below the tested devices in the measured frequency range.

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C.-Y. Chan, Y.-S. Lin, Y.-C. Huang, and S. S. H. Hsu are with the Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C. (e-mail: shhsu@ee.nthu.edu.tw).

Y.-Z. Juang is with the National Chip Implementation Center, Hsinchu 300, Taiwan, R.O.C.

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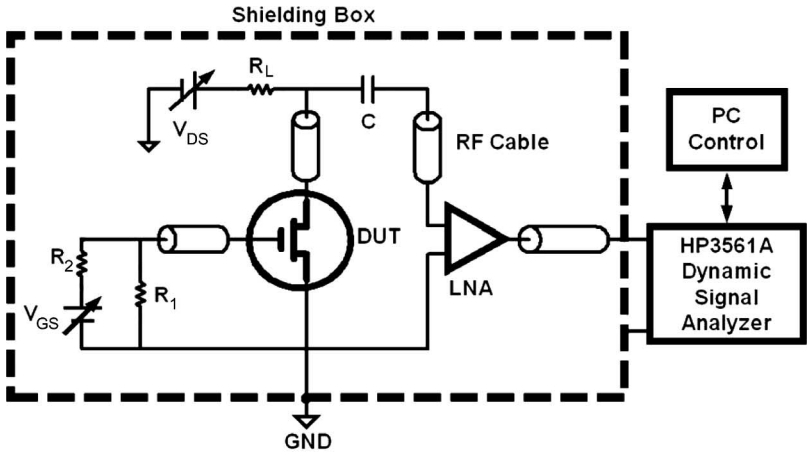
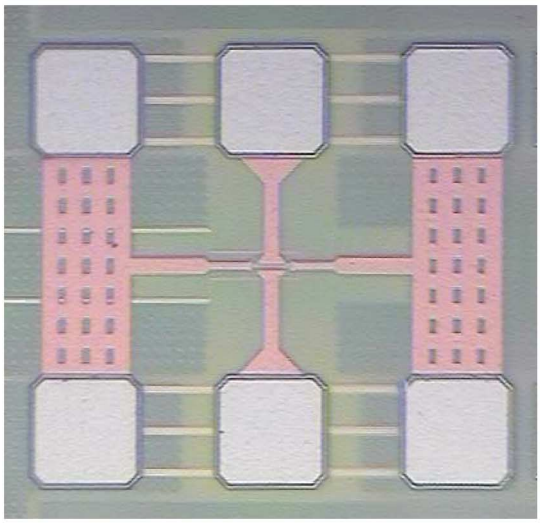


(a)



(b)

Fig. 1. (a) Flicker noise measurement setup. (b) Micrograph of a 0.13-μm RF NMOS with the G–S–G probing pads.

Fig. 1(b) shows the layout of the RF MOSFETs with ground–signal–ground (G–S–G) RF pads. Devices characterized in this paper were fabricated by a standard 0.13-μm CMOS process, with a gate oxide thickness of $\sim$27 Å and a threshold voltage of $\sim$0.4 V. For nanometer devices with very high low-frequency gain, using a well-grounded signal path including RF pads and the aforementioned system can effectively avoid the oscillation problem during the measurement to obtain reliable data [13]. The gate terminal was ac short-circuited through a large capacitor, and the drain current noise spectral density was measured. Note that the drain noise voltage spectral density was measured first, and then converted back to the drain noise current characteristics, as presented in the following sections. Devices with three different finger widths, including 1, 5, and 10 μm, and the corresponding finger numbers of 40, 8, and 4 were tested, which have the same total channel width of 40 μm for a fair comparison. To further study the noise origin, one-finger devices $(W = 10\ \mu\text{m})$ with different STI-to-gate distances SA(SB) of 0.6, 1.2, and 10 μm were also investigated. The results provide a direct evidence of the STI effect on the device flicker noise characteristics.

III. Results and Discussion

A. DC Characteristics

Five devices of each type on different chips were measured under a wide range of bias conditions for a more representative analysis on device flicker noise properties. Fig. 2 shows the dc current distribution for devices with various finger widths and numbers. As can be seen, the average drain current increased as the finger number decreased and the finger width increased. Also, the devices with $W = 1\ \mu$m $(N_{\text{finger}} = 40)$ presented a significantly wider variation than those with $W = 5\ \mu$m $(N_{\text{finger}} = 8)$ and $W = 10\ \mu$m$(N_{\text{finger}} = 4)$. The results can be attributed to the stress effect originating from the STI structure which can generate nonuniform compressive stress especially between the trench edge and the active region. As a consequence, the carrier mobility of electrons is reduced in nMOSFETs leading to a reduced drain current [1]–[3]. The results suggest that the devices with a smaller finger width (larger finger number) suffered more from the STI stress compression and present a smaller average drain current. In addition, these devices are more sensitive to the STI stress variation

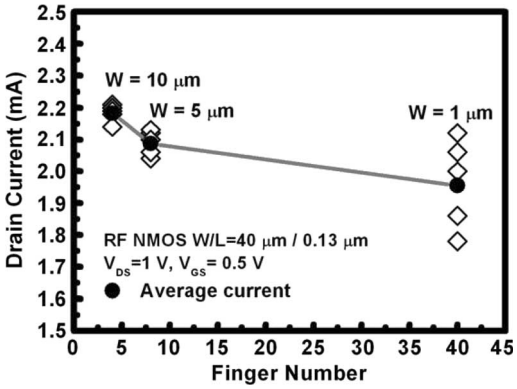


Fig. 2. Drain current variations as a function of the finger number and the width of each finger for 0.13-μm RF NMOS devices.

resulting in a larger distribution in the drain current. More discussions together with the noise characteristics and the dependence of device geometries will be carried out later.

B. Flicker Noise Characteristics

As mentioned above, the STI-induced compressive stress has a significant effect on carrier mobility and thus change the dc characteristics. It is also interesting to investigate if the stress has a direct impact on the flicker noise properties. It has been reported that both carrier number fluctuations ΔN and mobility fluctuations $\Delta\mu$ could be the possible reasons to explain the observed flicker noise in semiconductor devices [14]. In this case, although the electron mobility in the channel is affected due to the compressive stress from the STI region, one cannot conclude that the mobility fluctuations are responsible for the observed flicker noise characteristic. To identify the noise origin, the devices were characterized in the triode region. According to Ghibaudo *et al.* [14], [15], if the $S_{\rm ID}/I_2$ curve is well correlated with $(g_m/I)^2$, the noise characteristic tends to be carrier number fluctuations dominated, which can be described by the following equation:

$$\frac{S_{\rm ID}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{\rm fb}}(f) \tag{1}$$

where g_m is the gate transconductance, and $S_{V_{\rm fb}}$ is the flatband voltage spectral density. $S_{V_{\rm fb}}(f)$ can be expressed as [16]

$$S_{V_{\rm fb}}(f) = \frac{q^2 kT\lambda N_t(E_F)}{WLC_{\rm ox}^2}\frac{1}{f^\eta} \tag{2}$$

where k is the Boltzmann constant, T is the operating temperature, η is the slope of the frequency dependence, and N_t is the trap density. It can be seen in (2) that both trap density and distribution can affect the flicker noise characteristics.

Fig. 3(a) and (b) shows both $S_{\rm ID}/I^2$ at 10 Hz and $(g_m/I)^2$ as a function of the drain current for devices with $W = 10$ μm ($N_{\rm finger} = 4$) and $W = 5$ μm ($N_{\rm finger} = 8$), respectively. The devices were biased in the triode region under a fixed $V_{\rm DS}$ of 50 mV, and $V_{\rm GS}$ varied from 0.4 to 0.8 V (50 mV/step). As shown in the figures, the $S_{\rm ID}/I^2$ curve is in good agreement

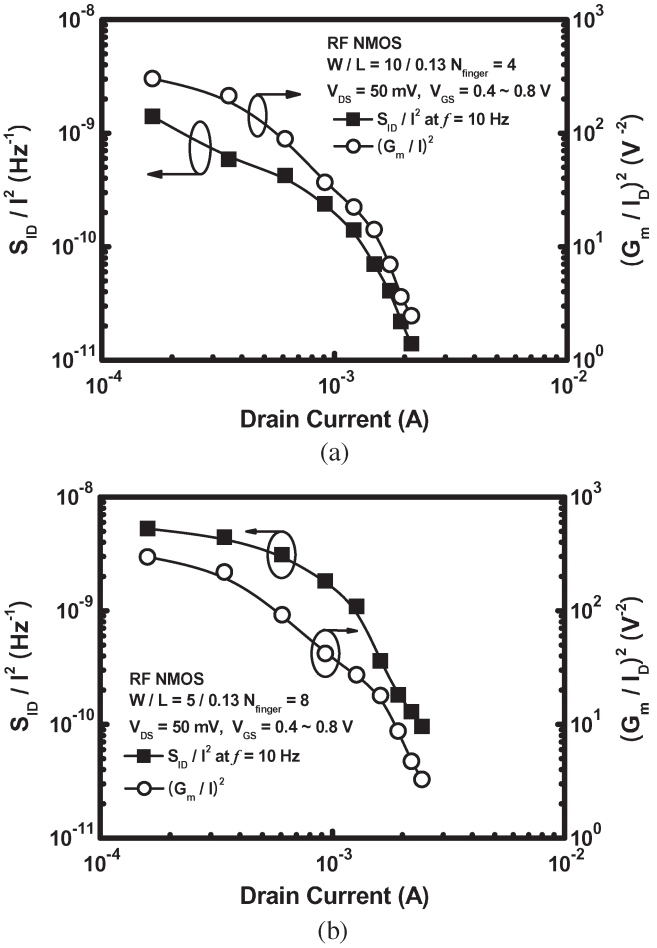


Fig. 3. Noise current spectral density $S_{\rm ID}/I^2$ at 10 Hz and the $(g_m/I_D)^2$ values as a function of the drain current for a 0.13-μm RF NMOS. (a) $W = 10$ μm ($N_{\rm finger} = 4$). (b) $W = 5$ μm ($N_{\rm finger} = 8$). Both are under a $V_{\rm DS}$ of 50 mV and a $V_{\rm GS}$ from 0.4 to 0.8 V (50 mV/step).

with $(g_m/I)^2$, which indicates that the noise characteristics can be better explained by the carrier number model.

Note that for devices with $W = 5$ μm ($N_{\rm finger} = 8$), as shown in Fig. 3(b), the $S_{\rm ID}/I^2$ values present a slight deviation from the $(g_m/I)^2$ curve under a strong inversion bias condition. The observed trend can also be explained by the carrier number model while including a correlated mobility scattering term, which can be described by the following equation [14]:

$$\frac{S_{\rm ID}}{I_D^2} = \left[1 \pm \alpha\mu_{\rm eff} C_{\rm ox}\frac{I_D}{g_m}\right]^2 \frac{g_m^2}{I_D^2} S_{V_{\rm fb}}(f) \tag{3}$$

where α is the scattering parameter, and $\mu_{\rm eff}$ is the effective carrier mobility. The measured results suggest that the correlated mobility scattering cannot be neglected for devices with a shorter finger width and more finger numbers. Additionally, by comparing Fig. 3(a) with Fig. 3(b), the devices with $W = 5$ μm ($N_{\rm finger} = 8$) show higher noise levels than those with $W = 10$ μm ($N_{\rm finger} = 4$).

Figs. 4–6 present the normalized drain noise current spectral densities in the saturation region for NMOS devices with $W = 1$ μm ($N_{\rm finger} = 40$), $W = 5$ μm ($N_{\rm finger} = 8$), and $W = 10$ μm ($N_{\rm finger} = 4$), respectively. The gate bias ($V_{\rm GS}$) varied

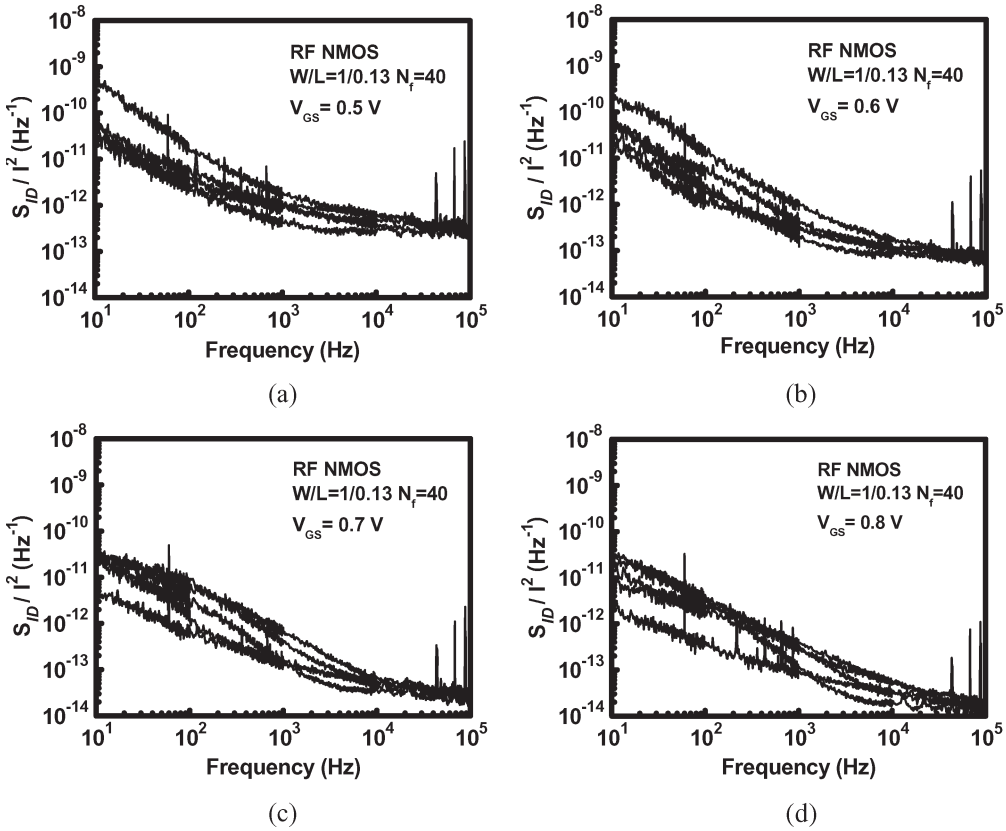


Fig. 4. Noise current spectral densities for a 0.13-μm RF NMOS with $W = 1\ \mu$m ($N_{\rm finger} = 40$) under a $V_{\rm DS}$ of 1.0 V and (a) $V_{\rm GS} = 0.5$ V, (b) $V_{\rm GS} = 0.6$ V, (c) $V_{\rm GS} = 0.7$ V, and (d) $V_{\rm GS} = 0.8$ V.

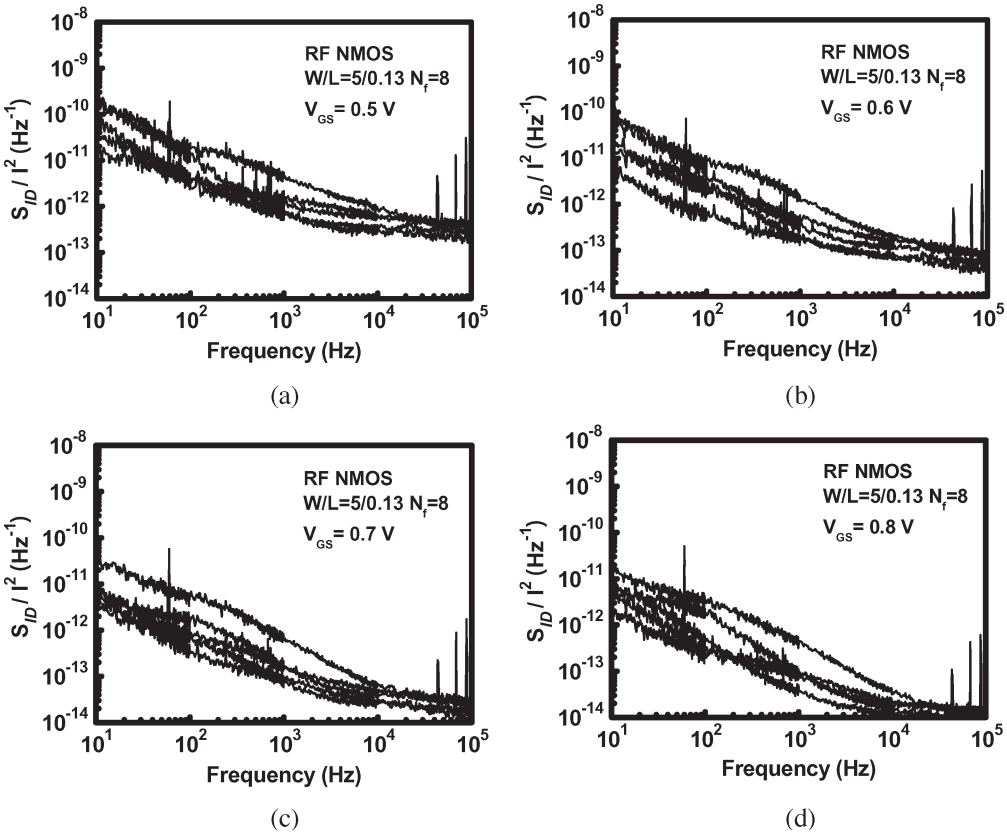


Fig. 5. Noise current spectral densities for a 0.13-μm RF NMOS with $W = 5\ \mu$m ($N_{\rm finger} = 8$) under a $V_{\rm DS}$ of 1.0 V and (a) $V_{\rm GS} = 0.5$ V, (b) $V_{\rm GS} = 0.6$ V, (c) $V_{\rm GS} = 0.7$ V, and (d) $V_{\rm GS} = 0.8$ V.

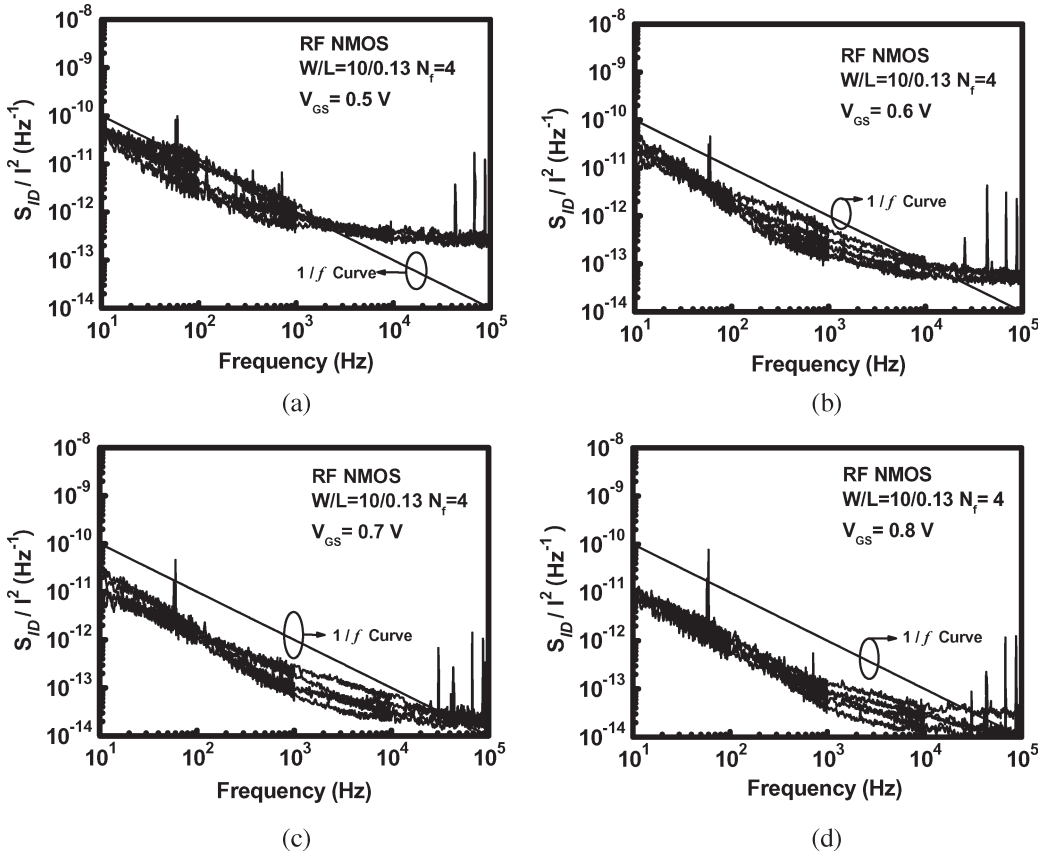


Fig. 6. Noise current spectral densities for 0.13-μm RF NMOS with $W = 10$ μm ($N_{\rm finger} = 4$) under a $V_{\rm DS}$ of 1.0 V and (a) $V_{\rm GS} = 0.5$ V, (b) $V_{\rm GS} = 0.6$ V, (c) $V_{\rm GS} = 0.7$ V, and (d) $V_{\rm GS} = 0.8$ V.

from 0.5 to 0.8 V under a fixed drain bias ($V_{\rm DS}$) of 1 V. As can be seen in both Figs. 4 and 5, the devices present a large variation of the noise levels and pronounced G–R noise components. However, an obviously smaller variation of flicker noise was obtained for the devices with $W = 10$ μm ($N_{\rm finger} = 4$), as shown in Fig. 6. Fig. 7 plots the noise current spectral densities at 100 Hz for the three types of devices under different gate biases. It can be seen that the devices with $W = 10$ μm ($N_{\rm finger} = 4$) presented a much smaller noise level variation and a lower average value compared to other geometries. The same trend was also found in Fig. 3, where $S_{\rm ID}/I^2$ for $W = 5$ μm ($N_{\rm finger} = 8$) devices presents a higher noise level than that with $W = 10$ μm ($N_{\rm finger} = 4$).

As mentioned, the devices with a smaller width but a larger $N_{\rm finger}$ suffered more nonuniform STI stress, which can cause variations of carrier mobility in the channel, leading to a drain current distribution as shown in Fig. 2. On the other hand, the analysis based on the measured results in Fig. 3 suggests that carrier number fluctuations are the main origin of the observed flicker noise characteristics. Therefore, the stress-induced mobility variation may not be directly responsible for the observed noise level deviation from chip to chip. However, the stress due to the abrupt transition between the STI and active region can induce traps during the process and still be an important factor for the observed strong geometry dependence of the flicker noise in these devices.

Fig. 8 is a conceptual plot of different device layouts to explain the observed trends, where the STI region, the high stress region, and the active region are indicated. Two extreme cases in this paper with $W = 10$ μm ($N_{\rm finger} = 4$) and $W = 1$ μm ($N_{\rm finger} = 40$) are shown in Fig. 8(a), where the arrows indicate the directions of the main compression stress in each device. Fig. 8(b) highlights the layer structure of the STI edge and possible locations of the traps. A transmission electron microscope (TEM) picture of defects focuses on the transition region between the STI and the active region, as shown in Fig. 9. As can be seen, defects can be clearly observed between STI and the active region.

For the devices with $W = 1$ μm, the carriers in the channel should suffer more stress from the y-direction than that from the x-direction, while it is the opposite condition for the device with $W = 10$ μm, as indicated in the figure. The measured results suggest that the effect of the x-axis force on a wide device with less finger number is not obvious as can be seen from both the dc and noise characteristics. On the other hand, the effect of STI on devices with $W = 1$ μm and 40 fingers could be twofold. First, the STI edges in the y-direction are very close to the center of the channel, therefore, the nonuniform stress can directly affect the channel carriers resulting in mobility reduction and variation for the dc current. Second, the sidewall and the edge of the STI have abundant traps, which are also close to the center of the channel and can affect the noise characteristics especially the G–R noise components. As a result, a higher effective trap density can be expected for devices with a shorter finger width and more finger numbers. In addition, it is more likely to have nonuniformly distributed stress and

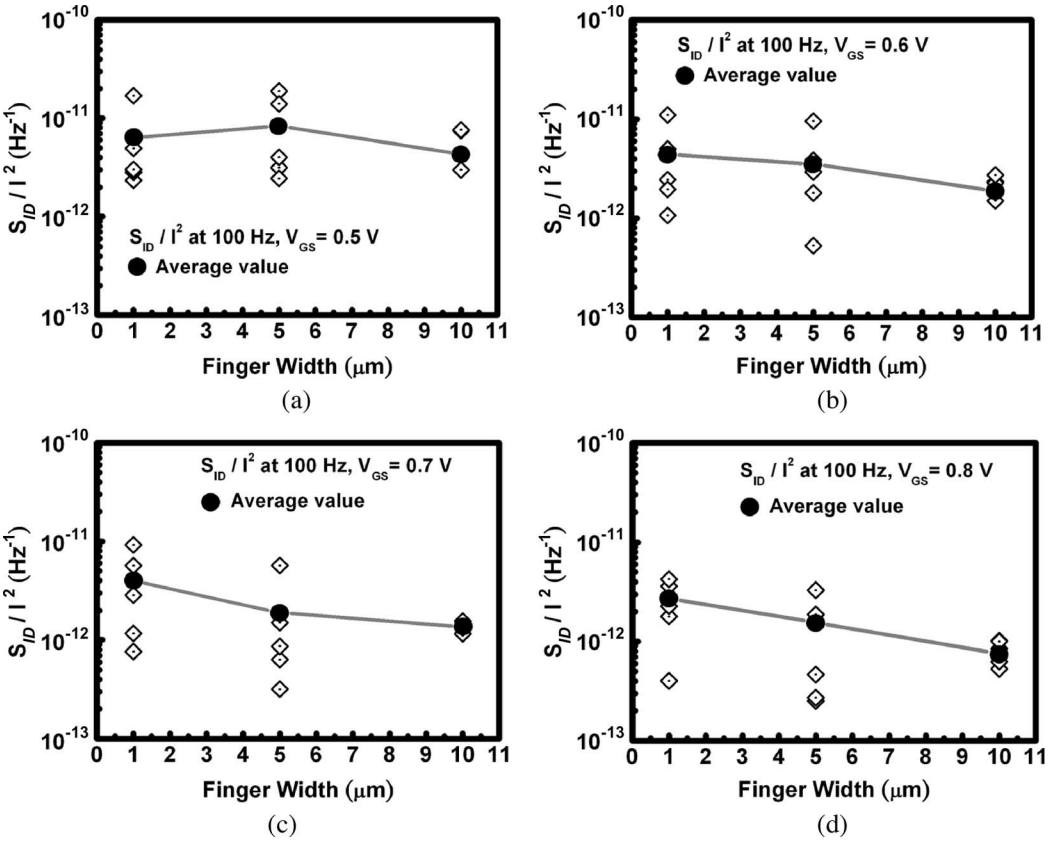


Fig. 7. Noise current spectral densities at $f = 100$ Hz as a function of the finger width under a $V_{\rm DS}$ of 1.0 V and (a) $V_{\rm GS} = 0.5$ V, (b) $V_{\rm GS} = 0.6$ V, (c) $V_{\rm GS} = 0.7$ V, and (d) $V_{\rm GS} = 0.8$ V.

thus the associated variation of the trap density in different devices [17].

Effects of increased noise variation have been reported by many researchers [10]–[12], [18], [19], which were mainly attributed to the appearance of the G–R centers associated from the scaling down of device geometry. In this paper, as the width of each gate finger reduces, the noise variation also increases. The observed trend was also attributed to the G–R centers, while the main reason is explained by the STI effect. To further confirm this point, one-finger devices with a finger width of 10 μm but various STI-to-gate distances were measured. As shown in Fig. 10(a), SA(SB) were designed as 0.6 (minimum rule), 1.2, and 10 μm, respectively. Fig. 10(b) shows the measured results. As the STI edge becomes very close to the gate, the noise level variation increases, which provides a direct proof of the STI effect on flicker noise characteristics. This point is different from the previously reported results, which attributed the noise variation mainly to the device scaling.

In addition, we found that the G–R humps shift slightly toward higher frequencies with increased $V_{\rm GS}$. In our discussion, the appearance of G–R humps was attributed to the structural defects at the interface between STI and the active region especially at the gate finger edge, rather than those in the substrate. As indicated in Fig. 8(b), the oxide edge suffers a more significant compressive stress and results in many traps and interface states congregated around the high stress region. These traps and defects could be affected by the gate voltage due to the gate fringing field, resulting in the gate-bias-dependent G–R humps.

To further investigate the observed G–R noise and the associated trap activation energy, flicker noise measurements under various temperatures were performed as described as follows.

C. Trap Activation Energy

Fig. 11(a) plots $f \times S_{\rm ID}$ of a $W = 1$ μm ($N_{\rm finger} = 40$) device with a clear bulge due to the G–R noise component. As can be seen, the corner frequency of the G–R noise shifted from $\sim$50 to $\sim$650 Hz as the temperature increased from 25 °C to 65 °C (10 °C/step). The observed characteristics can be explained by the carrier thermal energy and the trap potential well. With more kinetic energy as the temperature increases, the electrons become easier to be released from the potential well originated from the traps. As a result, the response time of the trapping/detrapping process reduces, and the G–R noise bulge moves toward higher frequencies. The trapping time constants can be extracted by fitting the measured data to an $1/f^{\eta}$ curve, together with a Lorentz component as follows:

$$S_{\rm ID} = \frac{K_1}{f^{\eta}} + \frac{4K_2\tau}{1+\omega^2\tau^2} \tag{4}$$

where K_1 and K_2 are fitting parameters, η is the slope of frequency dependence, τ is the trapping time constant, and ω is the angular frequency. By selecting proper values, a good agreement between the measured data and the curve described by the equation can be obtained. With the obtained time constants, the

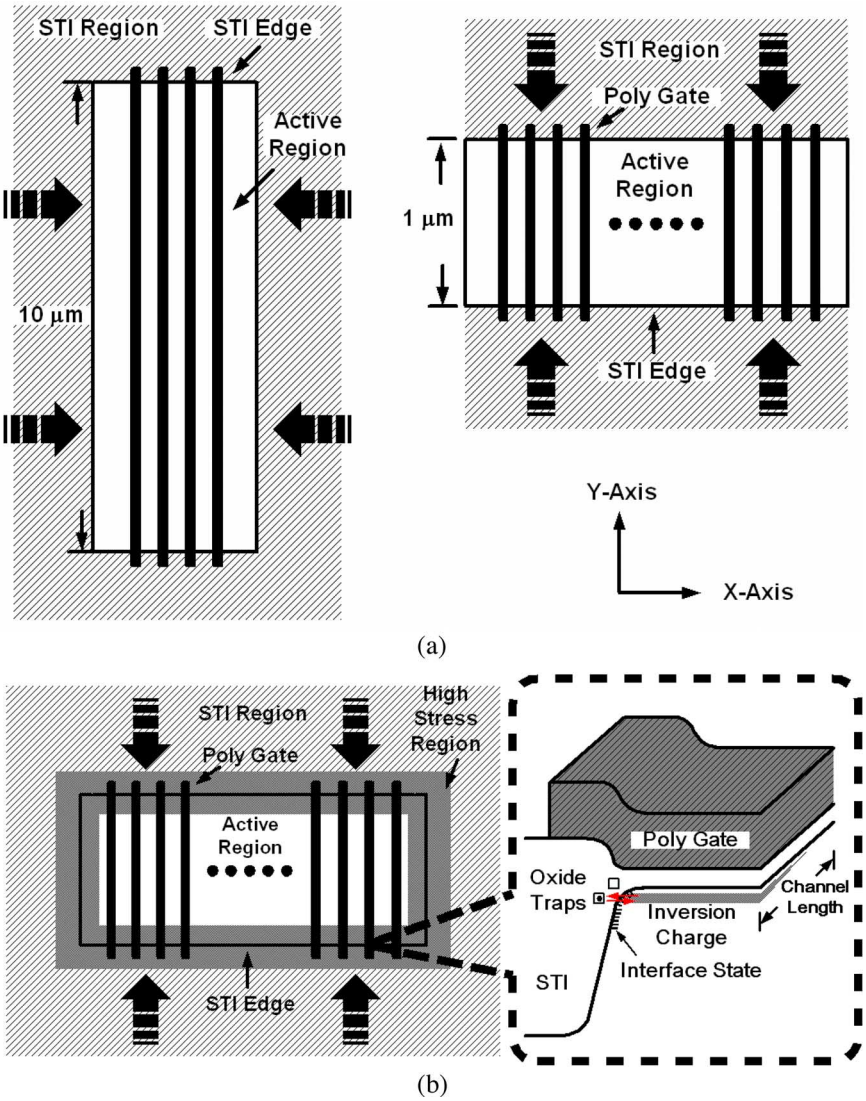


Fig. 8. (a) Conceptual device layouts for a 0.13-μm RF NMOS with $W = 10$ μm ($N_{\rm finger} = 4$) and $W = 1$ μm ($N_{\rm finger} = 40$). (b) Layer structure of the STI edge and possible locations of the traps.

Arrhenius relation can be used to determine the following trap activation energy [20]:

$$\ln(T^2\tau) = \frac{E_C - E_T}{k}\left(\frac{1}{T}\right) + \ln\left(\frac{1}{A\sigma_n}\right) \tag{5}$$

where A is a constant, τ is the emission times, σ_n is the electron capture cross sections, k is the Boltzmann constant, T is the operating temperature, and $(E_C - E_T)$ is the trap activation energy. By plotting $\ln(T^2\tau)$ as a function of $1/T$ (Arrhenius plot), the trap activation energy $(E_C - E_T)$ can be extracted from the slope as shown in Fig. 11(b). The values obtained from five different devices are 0.397, 0.54, 0.472, 0.42, and 0.535 eV, respectively. The obtained activation energies show a distribution of trap levels between different devices, which suggests that the origins of the observed G–R noise may not be attributed to a unique factor. As reported in [21]–[23], various activation energies of traps were also observed by measuring the test structures for MOS memory devices by the deep-level transient current spectroscopy measurements, which were also attributed to the interface states of the STI structure and also possibly the metal-introduced deep levels. Compared to the conventional local-oxidation-in-silicon process, modern CMOS technology uses STI as the isolation structure between devices, leading to a smaller distance between the high-stress region and the intrinsic device area. It can be foreseen that the impacts of the G–R centers introduced from the STI on flicker noise can be more severe as the technology continuously scales down.

D. Modeling the Variation in the Flicker Noise

To quantitatively study the noise level variation in different transistor geometries, the following formulas were employed to analyze the measured data. The relative standard deviation $\sigma_{\rm dB}$ can be calculated by [10]–[12]

$$\sigma_{\rm dB} = \sqrt{\frac{1}{N-1}\sum_{j=1}^{N}\left(S_{{\rm ID},j}\,|_{\rm dB} - \langle S_{\rm ID}\rangle|_{\rm dB}\right)^2} \tag{6}$$

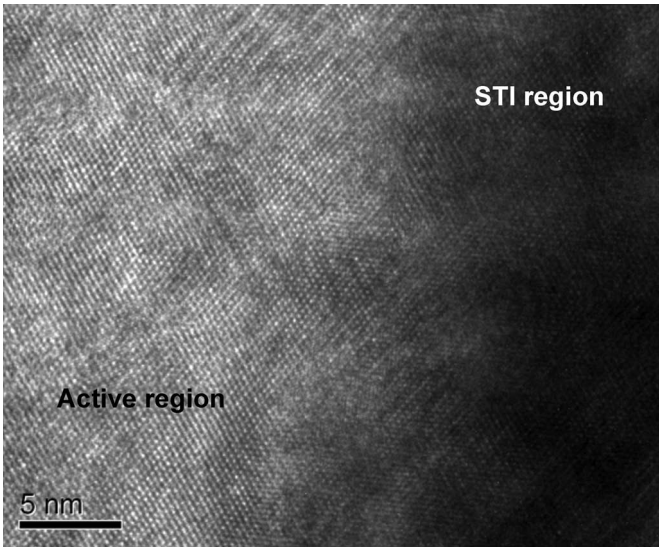


Fig. 9. TEM photograph of the interface between STI and the active region in the vicinity of a gate finger.

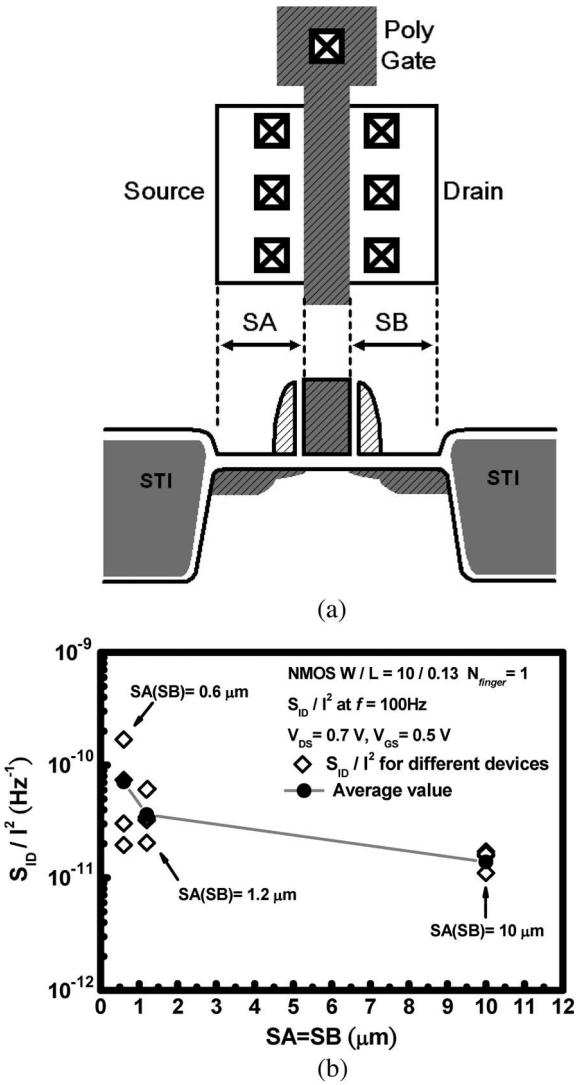


Fig. 10. (a) Device layout and cross section for an NMOS with $W/L = 10/0.13$ ($N_{\rm finger} = 1$). (b) Noise current spectral densities at 100 Hz for devices with SA(SB) = 0.6, 1.2, and 10 μm, respectively.

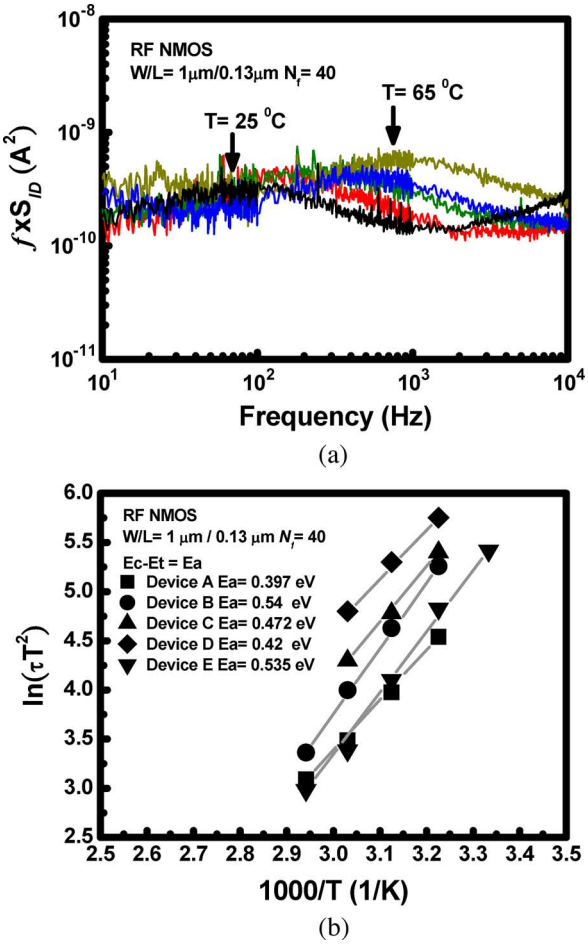


Fig. 11. (a) $f \times S_{\rm ID}$ of a 0.13-μm RF NMOS with $W = 1$ μm ($N_{\rm finger} = 40$). The G–R noise bulge shifts toward higher frequencies as the temperature increases from 25 °C to 65 °C (10 °C/step). (b) Corresponding Arrhenius plot of the 0.13-μm RF NMOS. The extracted trap activation energies are 0.397, 0.54, 0.472, 0.42, and 0.535 eV, respectively.

TABLE I
RELATIVE STANDARD DEVIATION $\sigma_{\rm dB}$ AND THE CORRESPONDING NOISE VARIATION LEVEL FOR DIFFERENT TYPES OF DEVICES

Device Size	$\sigma_{\rm dB}$	S_+
W/L=10/0.13 (N_{finger}= 4)	1.54	1.035
W/L=5/0.13 (N_{finger}= 8)	2.94	2.871
W/L=1/0.13 (N_{finger}= 40)	2.95	2.893

where $S_{{\rm ID},j}$ is the jth spectrum, $S_{{\rm ID},j}|_{\rm dB} = 10 \times \log(S_{{\rm ID},j})$, and $\langle S_{\rm ID} \rangle$ is the average noise level. For devices with $W = 1$ μm ($N_{\rm finger} = 40$), $W = 5$ μm ($N_{\rm finger} = 8$), and $W = 10$ μm ($N_{\rm finger} = 4$), the calculated $\sigma_{\rm dB}$ were 2.95, 2.94, and 1.54 dB, respectively. As expected, the $W = 10$ μm devices resulted in the smallest $\sigma_{\rm dB}$.

For a simplified analysis, the relative noise level and noise model can be described as follows:

$$S_{\rm ID} = \frac{K_F I_D^{AF}}{f} \times (1 + S_{\pm}) \tag{7}$$

where S_+ and S_- are the relative noise variation levels above and below the average noise $\langle S_{\rm ID} \rangle$. The variations can be

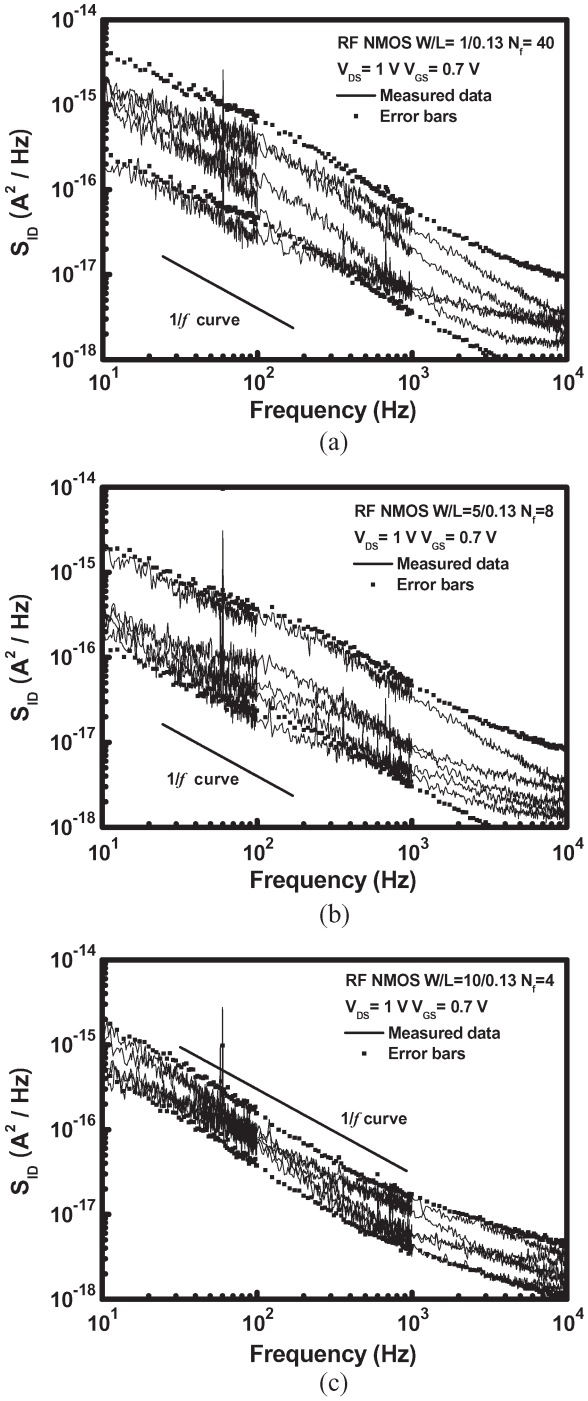


Fig. 12. Current noise spectral (solid line) and error bars (dotted line) for a 0.13-μm RF NMOS with (a) $W = 1$ μm ($N_{\rm finger} = 40$), (b) $W = 5$ μm ($N_{\rm finger} = 8$), and (c) $W = 10$ μm ($N_{\rm finger} = 4$), using $k = 2$.

determined from $\sigma_{\rm dB}$ by

$$S_{\pm} = 10^{\pm k\sigma_{\rm dB}/10} - 1 \tag{8}$$

where the constant k depends on the confidence probability selected. The calculated $\sigma_{\rm dB}$ and the corresponding S_+ (using $k = 2$) are listed in Table I. As can be seen, S_+ slightly decreased as the finger length increased from 1 μm($N_{\rm finger} = 40$) to 5 μm ($N_{\rm finger} = 8$). However, a significant improvement of S_+ was obtained as the finger length increased to 10 μm ($N_{\rm finger} = 4$). Fig. 12 presents the measured results and the error bars (dotted lines) for the three types of devices.

Finally, an important point that have to be addressed from the RF circuit design consideration is that RF MOS devices are typically designed with multiple fingers with a relatively small finger width to reduce the gate resistance for optimized high-frequency characteristics. For example, a 100×1 μm$/0.13$ μm NMOS transistor has been reported for $f_{\rm max}$ of 135 GHz [24]. However, a large deviation due to the impact of STI effect can be expected in both dc and noise characteristics for such a device design approach based on the above discussion, which can be a serious problem for circuit applications.

IV. Conclusion

In this paper, the impacts of STI on flicker noise in 0.13-μm RF NMOS have been investigated. For devices with the same W/L ratio, the devices with more fingers and a smaller width presented a wider variation in both dc current and noise characteristics. More pronounced G–R components and higher noise levels were also observed in these devices. The results indicated that the compressed STI stress has a higher impact on these devices, resulting in nonuniformly reduced carrier mobility from different chips. In addition, the nonuniformly distributed traps located at the finger edge between STI and the active region are the main origin for the observed flicker noise characteristics, which can be better explained by the carrier number fluctuations with correlated mobility scattering. Finally, modeling of the noise level variation in this paper provided quantitative analysis of these devices, which can be incorporated in SPICE model for circuit design applications.

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Chih-Yuan Chan was born in Kaohsiung, Taiwan, R.O.C., in 1979. He received the M. S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 2003, where he is currently working toward the Ph.D. degree.

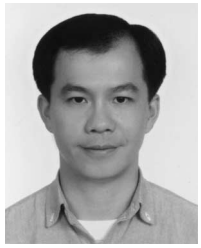
His current research interests include CMOS design and characterization for microwave applications, including layout optimization, characterization, and modeling of flicker noise and high-frequency noise and RF measurement and deembedding techniques.

Yu-Syuan Lin was born in Changhua, Taiwan, R.O.C., in 1981. He received the B. S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 2003, where he is currently working toward the Ph.D. degree in the Institute of Electronics Engineering.

His current research interests include design and fabrication of III-nitride-based devices for high-power and high-speed applications. His work also involves device characterization and reliability analysis.

Yen-Chun Huang was born in Tainan, Taiwan, R.O.C., in 1983. He received the B.S. and M.S. degrees from National Tsing Hua University, Hsinchu, Taiwan, in 2005 and 2007, respectively.

He is currently with the Institute of Electronics Engineering, National Tsing Hua University. His research mainly focuses on flicker noise characterization and modeling of RF CMOS devices.



Shawn S. H. Hsu (M'04) was born in Tainan, Taiwan, R.O.C. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, the M.S. degree from the University of Michigan, Ann Arbor, in 1997, and the Ph.D. degree in 2003.

He joined the III–V Integrated Devices and Circuits Group at the University of Michigan in 1997. From 1992 to 1994, he served as a lieutenant in the Army. From 1994 to 1995, he was a Research Assistant at the National Chiao Tung University, Hsinchu. He is currently an Associate Professor in the Institute of Electronics Engineering, National Tsing Hua University. His current research interests include the analytical and empirical large-signal and noise modeling of Si/III–V-based devices for RFIC/MMIC design applications, the implementation and development of various measurement techniques to extract parameters for equivalent circuit models, and the design of MMICs and RFICs using Si/III–V-based devices for low-noise, high-linearity, and high-efficiency system-on-chip applications.

Ying-Zong Juang received the M.S. and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1992 and 1998, respectively.

He joined the National Chip Implementation Center (CIC), Science-Based Industrial Park, Hsinchu, Taiwan, in October 1998. At CIC, he worked on RF circuit design and device modeling; furthermore, from 1999 to 2000, he joined a project to create a new process flow to implement the BCD devices on the same chip. He is currently a Researcher and the Director of the Chip Implementation Service Department, CIC, where he organizes several projects, including top-down design platforms for RF transceivers and 0.35-μm/0.18-μm CMOS/MEMS design environments. His research interests include RF/MEMS module design, CMOS BioMEMS, and mixed-signal design for RF front-end.