Substrate Noise Coupling Reduction in LC Voltage-Controlled Oscillators

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***Abstract*—In this letter, a substrate noise coupling effect in LC voltage-controlled oscillators (VCOs) was investigated. By 0.18-μm CMOS technology, three 2.4-GHz VCOs were designed using different types of spiral inductors to observe the substrate noise induced spurs. Compared with the design using a standard inductor, the proposed deep N-well (DNW) and patterned ground shield (PGS) VCOs demonstrated clearly reduced third-order intermodulation spurs by 6–8 and 10–15 dB, respectively. Based on the established physical-based equivalent circuit models, we found that the low-impedance paths introduced by DNW and PGS were the dominant factor for the observed substrate noise reduction in the proposed VCOs.**

***Index Terms*—Integrated circuits, noise.**

I. Introduction

CONTINUOUS scaling of CMOS transistors increases the operation frequency and the integration level of circuits rapidly. However, substrate noise coupling effect has become a major obstacle for this trend and can no longer be neglected [1]–[3]. In many highly integrated chips for communications, one of the most sensitive circuits is the voltage-controlled oscillator (VCO), which is often a key component in phase-locked loops and frequency synthesizers. Substrate noise coupling effect in LC VCOs and RF receiver circuits has been investigated using various approaches [4]–[8]. One important conclusion is that the spiral inductor, owing to the relatively large area, is an important origin to pick up the substrate noise from the adjacent circuit blocks. With the metal interconnects linked to the transistors and varactors, the noise collected by the inductor can be an important contributor to the undesired spurs in addition to the direct coupling through the body of the nonlinear devices.

In this letter, three LC VCOs with the same core circuit but different spiral inductors are realized in 0.18-μm CMOS technology. In addition to the standard inductor provided by the foundry, two different designs, including deep N-well (DNW) and patterned ground shield (PGS), are utilized to improve the isolation of substrate noise. Both second-order (IM2) and third-order (IM3) intermodulation spurs are investigated using externally injected noise. The observed trends are also analyzed by the inductor equivalent circuit models.

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II. VCO Design for Low Substrate Noise Coupling

A. Inductor Design

Fig. 1 shows the different inductors and the corresponding equivalent circuit models of the substrate. As indicated by the dashed-line box in Fig. 1(a), the spiral inductor with the P+ guard ring is the foundry standard design. With the metal one layer (M1) connected to the substrate through the P+ contact, the noise generated from the adjacent aggressors can be guided to the ground to prevent the interference. However, the undesired noise signal may still propagate through the substrate and reach the inductor particularly from the large bottom area.

A straightforward solution is to use a DNW layer to prevent the noise coming from the substrate. The DNW structure has been widely used to reduce undesired interference [9]–[11]. As shown in Fig. 1(a), the DNW/NW structure completely surrounds the substrate underneath the inductor and enhanced noise isolation can be expected. Another structure, PGS, is also employed to reduce the substrate noise coupling. With the metal strips placed underneath the inductor, the PGS structure has been used to increase the inductor quality factor, owing to the reduced image current [12]. Previous studies showed the benefit of using DNW and PGS in reducing substrate noise coupled into inductors [9]–[12]. In this letter, we further investigate these inductors in VCO circuits for substrate noise isolation.

B. VCO Design and Noise Injection

The 2.4-GHz VCOs designed in this letter employ the complementary cross-coupled topology for high output swing and low phase noise. The three inductors have the same top layer (Metal 6) geometry. The P+ guard ring, DNW, and PGS are connected to the VCO ground in each design. Although the peak Q values are different, the inductors are carefully designed to have similar Q and inductance ($\sim$7.0 and $\sim$2.5 nH, respectively) in the desired frequency range, which results in almost identical characteristics of the three VCOs. The measured phase noise is -125 dBc/Hz (1-MHz offset), and the power dissipation is 11.5 mW under a 1.6-V power supply. The tuning range is from 2.0 to 2.6 GHz.

The substrate noise was imitated by injecting a signal on-wafer directly using the ground-signal-ground RF probe. The distance from the injection pads to the center of the inductors is 350 μm. The signal pad is connected from the top metal layer M6 to the substrate P+ contact, whereas the two ground pads are connected only from M6 to the second metal layer M5. The somewhat "floated" grounds can prevent a short-distance return

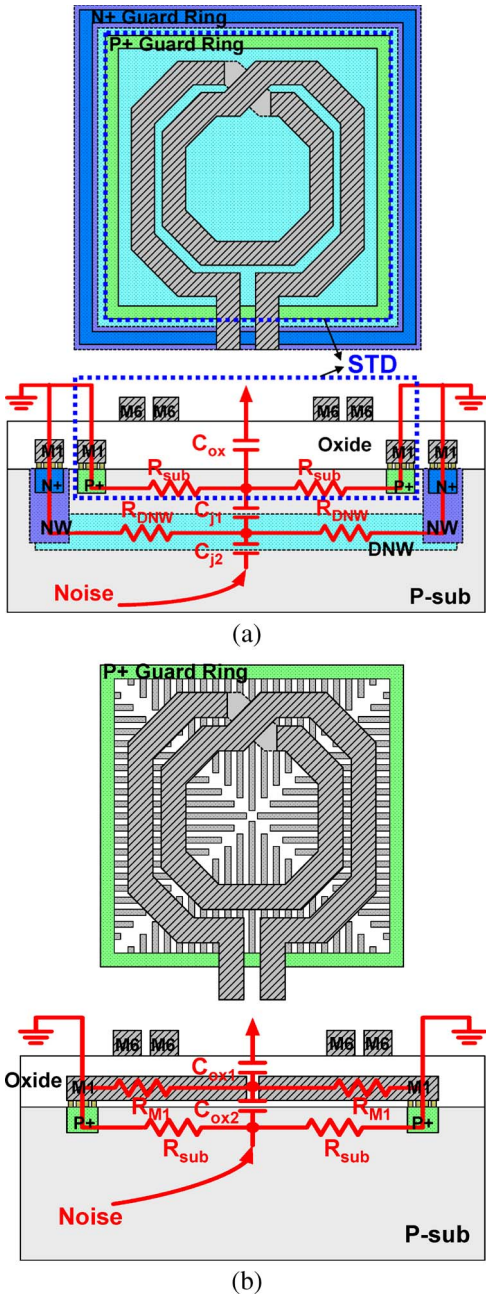

Fig. 1. Top views, cross sections, and the corresponding equivalent circuit models of (a) standard/DNW inductor and (b) PGS inductor.

path and ensure that the noise signal injects into the silicon substrate [4].

III. Experiment Results and Discussion

Considering a two–tone input signal (f_1 and f_2) for a nonlinear circuit, the output spectrum consists of harmonics of the form

$$mf_1 + nf_2 \tag{1}$$

where $|m| + |n|$ is defined as the order of the intermodulation product $(m, n = 0, \pm 1, \pm 2, \ldots)$. Among these combinations, we are particularly interested in those located close to the

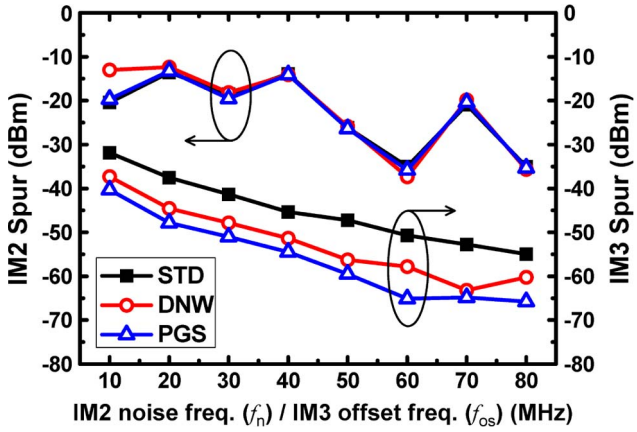

Fig. 2. Measured VCO IM2 and IM3 spurs under a 20-dBm external noise injection at $V_{\rm tune} = 0$ V.

oscillation frequency f_0, which can severely degrade the VCO performance. Assuming that f_0 and f_n (the injected noise frequency) are the two tones, the generated IM2 spurs $(f_0 \pm f_n)$ will be close to f_0 if f_n is a low-frequency signal. Similarly, certain IM3 spurs ($2f_0 - f_n$ and $2f_n - f_0$) can also appear at around f_0 if f_n is close to f_0. At $f_0 = 2.6$ GHz, Fig. 2 shows the measured IM2 $(f_0 + f_n)$ and IM3 ($2f_0 - f_n$, offset frequency $f_{\rm os}$ defined as $f_n - f_0$) plotted as a function of f_n and $f_{\rm os}$, respectively, under a noise level of 20 dBm. Although not shown here, the spur presents a linearly increased characteristic with the injected power within the measured range of -20–20 dBm. Interestingly, similar IM2 spurs among the three designs are observed. However, the VCOs using the DNW and PGS inductors demonstrate clearly reduced IM3 spurs by about 6 and 10 dB (at 30-MHz offset and $V_{\rm tune} = 0$ V), respectively. As $V_{\rm tune}$ varies from 0 to 1.6 V, the spur reduction ranges from 6 to 8 dB and 10 to 15 dB (at 30-MHz offset) for the DNW and PGS designs, respectively. The somewhat nonmonotonically dependence of IM2 on noise frequency f_n can be attributed to the floated ground pads for noise injection [4].

As shown in Fig. 1, a simple model is applied for the standard inductor, where $C_{\rm ox}$ describes the oxide parasitic capacitance underneath the inductor and $R_{\rm sub}$ models the substrate resistance of the P-sub layer. For the DNW case, the additional C_{j1} and C_{j2} describe the top and bottom parasitic junction capacitances, respectively, and $R_{\rm DNW}$ models the resistance of the DNW layer. For the PGS design, R_{M1} describes the resistance of the PGS constructed by the M1 layer, and $C_{\rm ox}$ is divided into two parts, $C_{\rm ox1}$ and $C_{\rm ox2}$, to be consistent with the physical structure. These capacitances can be easily estimated based on the physical parameters. Note that the impedance of the substrate is frequency dependent and the cutoff frequency can be estimated by [9]

$$f_c = \frac{\sigma_{\rm sub}}{2\pi\varepsilon_{\rm Si}} \tag{2}$$

where $\sigma_{\rm sub}$ is the substrate conductivity and $\varepsilon_{\rm Si}$ is the dielectric constant of silicon. As long as $\sigma_{\rm sub} \gg \omega\varepsilon_{\rm Si}$, the capacitive behavior is insignificant and the signal transmission will be dominated by the substrate's resistive nature. Therefore, it is

appropriate to use only $R_{\rm sub}$ and $R_{\rm DNW}$ to model the substrate here (for $1/\sigma_{\rm sub} = 10\ \Omega \cdot$ cm, $f_c \sim 15$ GHz).

On the other hand, the resistive components $R_{\rm sub}$, $R_{\rm DNW}$, and R_{M1} are much more difficult to be determined. A qualitative comparison is employed here for the following analysis, which will be verified later based on the extracted model parameters. Compared with the P-type substrate, it is reasonable to assume that the DNW layer has a higher conductivity due to the higher doping concentration and higher mobility, which implies that $R_{\rm DNW}$ is smaller than $R_{\rm sub}$. Moreover, R_{M1} should be much smaller than $R_{\rm DNW}$ and $R_{\rm sub}$, owing to the metal layer M1 used for the PGS structure.

The calculated results indicate that $C_{\rm ox}$ is about two orders of magnitude smaller than the junction capacitances C_{j1} and C_{j2} ($C_{\rm ox} = 135$ fF, $C_{j1} = 15$ pF, and $C_{j2} = 17$ pF). For the IM2 tests with injected noises in the megahertz range, the small $C_{\rm ox}$ dominates the overall impedance of the noise signal path from the substrate to the inductor, which acts as an open circuit to block the noise picked up from the spiral inductor. This also explains that the low–impedance paths underneath the inductors provided by $R_{\rm DNW}$ and R_{M1} do not play an important role here. Consequently, the IM2 spurs are mainly induced from the substrate coupling effect through the transistors and varactors, and the three VCOs with the same $C_{\rm ox}$ layer and the same core circuit present similar IM2 levels.

For the IM3 measurements with injected noises in the gigahertz range, the noise blocking function through the oxide layer reduces significantly and the effect of the DNW and PGS structures appears. In the DNW case, one may speculate that the additional p-n junction capacitances contribute to the observed better noise isolation. However, the aforementioned analysis suggests that since even $C_{\rm ox}$ is no longer effective, C_{j1} and C_{j2} with much larger values and thus much lower impedances should not be the dominant factor here. Instead, with the low–impedance path through $R_{\rm DNW}$ to guide the noise to the ground, the DNW design shows an obvious reduction of the IM3 spurs. This explanation is also consistent with the PGS case. As shown in Fig. 1(b), the patterned ground provides a signal path with an extremely low resistance R_{M1} to direct the noise to the ground, which leads to a significantly reduced IM3 spur. For a more complete noise coupling analysis based on the proposed equivalent circuit models, the substrate resistances in each case were extracted by fitting with the measured IM3 data. The obtained values of $R_{\rm sub}$, $R_{\rm DNW}$, and R_{M1} are 650, 450, and 0.05 Ω, respectively. The result is consistent with our prediction of $R_{\rm sub} > R_{\rm DNW} \gg R_{M1}$.

IV. Conclusion

In this letter, we proposed two approaches to reduce substrate noise coupling effect in VCOs. The measured results demonstrated that the IM3 spur was reduced by 6–8 dB with the DNW guard ring, and by 10–15 dB with the PGS inductor. Physical–based substrate equivalent circuit models of the spiral inductors were established to explain the observed trends. It was found that the additional low–impedance paths can direct the substrate noise signal to the ground, resulting in the reduced spurs. The proposed design concepts can be easily implemented in the standard CMOS process, which can be very useful to improve the substrate noise coupling effect in an LC VCO, particularly in a highly integrated chip with both digital and analog blocks for communications.

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