Wiring Effect Optimization in 65-nm Low-Power NMOS

Chih-Yuan Chan, San-Chuan Chen, Ming-Hsien Tsai, and Shawn S. H. Hsu

***Abstract*—This letter investigates the wiring effect on RF performance in advanced 65-nm low-power CMOS technology. New designs are proposed to minimize the parasitic resistances and capacitances associated with the interconnects in the transistor. Compared with the standard multifinger devices provided by the foundry, the device with the optimized wiring parasitic capacitances and resistances presents improvement up to ∼21% for f_T (increased from 89 to 108 GHz) and ∼22% for $f_{\max}$ (increased from 130 to 159 GHz), respectively. The extracted equivalent circuit model parameters indicate that the proposed approach can effectively minimize the parasitic effects leading to improved RF performance of the advanced MOSFETs.**

***Index Terms*—Layout, microwave transistors, millimeter-wave devices, semiconductor device modeling.**

I. Introduction

CONTINUOUS scaling of the gate length has made CMOS technology popular for high-speed circuit applications and impressive cutoff frequency (f_T) and maximum oscillation frequency ($f_{\max}$) have been achieved using advanced CMOS technology [1], [2]. In addition to process optimization, the device geometry and layout play a critical role to enhance the transistor RF performance [3]–[8]. Nicolson and Voinigescu [3] studied the MOSFETs with different gate connections. As device scaling down, the impact of finger length on high-frequency characteristics has been discussed [4], [5]. Tatsumi [6] and A. Nakamura *et al.* [7] also proposed the layout optimization of MOSFETs by TCAD simulations. Recently, a new layout design using 90-nm CMOS process was proposed to realize millimeter-wave circuits [8]. In this letter, new layout approaches are proposed to improve the transistor RF performance in 65-nm NMOS. This letter specifically focuses on the impacts of wiring effect on the corresponding parasitic capacitances and resistances. By changing the source, drain, and gate interconnects in the transistor, the capacitive and resistive parasitics can be reduced effectively, leading to improved cutoff frequency f_T and maximum oscillation frequency $f_{\max}$.

II. Transistor Design

Fig. 1 shows the typical (Device A) and proposed layouts (Devices B and C) of multifinger RF MOSFETs in 65-nm low-power technology with one poly- and six metal layers (1P6M). The source and drain for Device A are connected to metal four (M4) and metal two (M2), respectively, and the gate polylayer is connected to metal three (M3). The meander-type gate is employed to reduce the gate resistance owing to the parallel configuration. However, the sidewall overlaps, resulting from the multiple interconnect metal layers, may generate significant parasitic capacitances, as shown in the cross section along $A-A'$, where the drain node is surrounded by the gate interconnect layer leading to a large undesired parasitic gate–drain capacitance.

The proposed ring-type gate structure (Device B) uses only the polylayer for the gate. By removing the gate metal interconnects (M1 to M3), a much lower sidewall gate–drain capacitance can be expected, which can be understood by comparing the cross sections along $A-A'$. This design also has a reduced gate–source capacitance compared with that in Device A, which can be understood by $B-B'$. Note that Devices A and B have the same cross sections along $C-C'$. To further investigate the impact of vias and metal layers on the RF performance, the source and drain of Device C are connected only to M2 and M1, respectively. Along $C-C'$, the reduced vias and metal layers compared with Device A (Device B) result in less parasitic source resistances, which can increase the drain current and transconductance, leading to better RF performance. Additionally, the sidewall coupling capacitances may reduce, whereas those from the top-source metal may increase due to the smaller distance between M2 and the polygate, which is also shown in Fig. 1. A detailed analysis in each case will be discussed, together with the measurement results and the extracted small-signal model parameters, in the next section.

III. Results and Discussion

The devices characterized in this letter were fabricated by a low-power 65-nm CMOS process, which had an oxide thickness of ∼26 Å and a $V_{\rm th}$ of ∼0.5 V. Note that this process was optimized for low leakage current to achieve low power consumption with a relatively higher $V_{\rm th}$. Therefore, compared with the standard high-speed process, this technology shows a smaller current drive capability, current gain, and also a lower f_T. For a fair comparison, all device sizes are fixed as $W/L = 1\ \mu\text{m}/0.07\ \mu\text{m}$ ($N_{\rm finger} = 40$) and biased under $V_{\rm DS} = 1.2$ V, $V_{\rm GS} = 0.7$ V. To obtain a statistical conclusion, all the results presented in the following are the averaged values from five different devices. The “open-short” deembedding technique was employed [9], and the structures

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The authors are with the Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 300, Taiwan, R.O.C. (e-mail: shhsu@ee.nthu.edu.tw).

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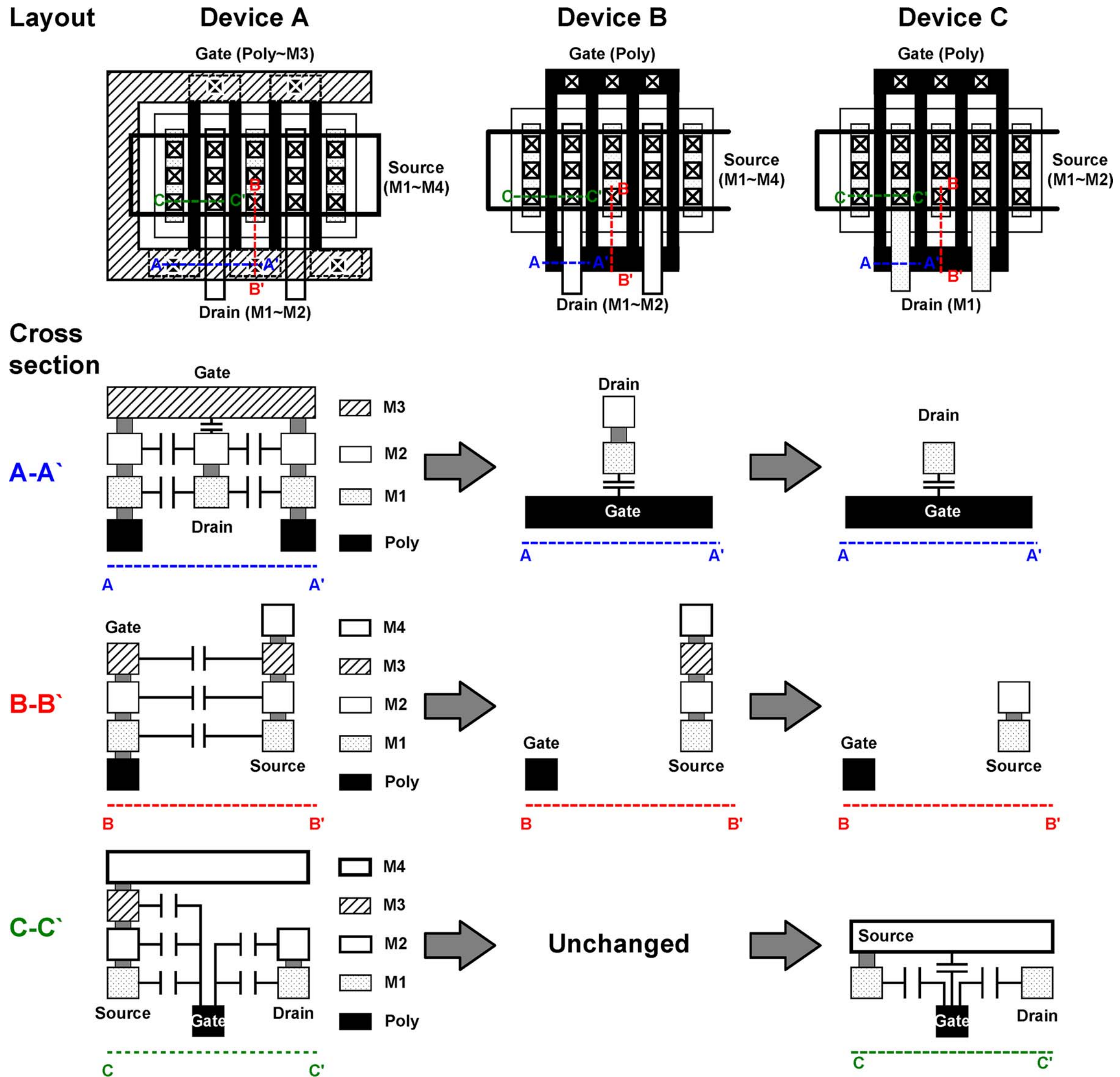

Fig. 1. Typical layout (Device A) and proposed ring-type polygate layouts (Devices B and C) for 65-nm RF MOSFETs. The step-by-step cross sections of $A-A'$, $B-B'$, and $C-C'$ illustrate the reduction of parasitics in the proposed designs.

are with different reference planes depending on the device layout. For example, the deembedding structure of Device A was connected from M6 to M4, whereas it was from M6 to M3 for Device C. In addition, the device reliability has been considered in the proposed designs. Considering that the drain uses only M1 in Device C, the maximum allowed current is approximately half of that in Devices A and B. Under a typical bias condition, the current flowing through the drain metal wire is below 2 mA (per micrometer width) for Device C, which is only ∼40% of the foundry-suggested value for safe operation at 100 °C. Therefore, the process reliability caused by high current densities should not be a major concern here.

The f_T and $f_{\max}$ of RF devices can be estimated by the equivalent circuit model parameters as follows (simplified from [5]):

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{\mathrm{gs}} + C_{\mathrm{gd}}} \tag{1}$$

$$f_{\max} = \frac{f_T}{2\sqrt{(R_g)(g_{\mathrm{ds}} + 2\pi f_T C_{\mathrm{gd}})}} \tag{2}$$

where g_m is the transconductance; C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances, respectively; R_g is the gate resistance; and g_{ds} is the output conductance. More discussion about f_T and $f_{\max}$ will be carried out together with these equations.

A. Small-Signal Parameters' Extraction

For quantitative analysis, C_{gs}, C_{gd}, and R_g are extracted based on the following [10], [11]:

$$C_{\mathrm{gs}} = \frac{\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}]}{\omega} \tag{3}$$

$$C_{\mathrm{gd}} \frac{-\mathrm{Im}[Y_{12}]}{\omega} \tag{4}$$

$$R_g = \frac{\mathrm{Re}[Y_{11}]}{(\mathrm{Im}[Y_{11}])^2}. \tag{5}$$

The values of C_{gs}, C_{gd}, and R_g listed in Table I were extracted from S parameters and averaged in a range from

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TABLE I
DESCRIPTION OF 65-nm NMOS WITH DIFFERENT LAYOUTS, INCLUDING METAL LAYERS, EXTRACTED PARASITIC CAPACITANCES, AND GATE RESISTANCES; DC CURRENT AND TRANSCONDUCTANCE; AND RF PERFORMANCE (AT $V_{\rm GS} = 0.7$ V AND $V_{\rm DS} = 1.2$ V)

65-nm Technology	*Device A*	*Device B*	*Device C*
Gate	Poly ~ M3	Poly	Poly
Source	M1~M4	M1~M4	M1~M2
Drain	M1~M2	M1~M2	M1
C_{gs} (fF)	34.4	30.5	30.2
C_{gd} (fF)	16.1	13.0	12.7
C_{total} (fF)	50.5	43.5	42.9
I_{DS} (mA)	4.8	4.8	5.1
g_m (mS)	30.4	30.4	31.2
R_g (Ω)	3.68	4.02	4.33
f_T (GHz)	89	102	108
f_{max} (GHz)	130	155	159

5 to 15 GHz, and $C_{\rm total}$ equals $C_{\rm gs} + C_{\rm gd}$. Compared with that in Device A, $C_{\rm total}$ reduced by ~14% for Device B. Additionally, the extracted $C_{\rm gs}$ and $C_{\rm gd}$ of Device C are similar to those of Device B. As mentioned earlier, the reduced sidewall capacitances are somehow compensated by the increased parasitic capacitance from the top-source metal in Device C, leading to a similar $C_{\rm total}$ with Device B. One point worth mentioning is that by removing the additional metal layers, the drain current $I_{\rm DS}$ in Device C increased by ~6%, and g_m increased by ~3% compared with that in Device B, which is also consistent with our prediction. Moreover, it should be noticed that the extracted R_g for Devices B and C increases slightly compared with Device A. This can be attributed to the resistivity of the polylayer, which is higher than that of the metal wire.

B. Cutoff Frequency

Fig. 2 shows the short-circuited current gain (H_{21}) and the maximum stable gain (MSG) versus the frequency for Devices A, B, and C, where a -20 dB/dec extrapolation is employed beyond 110 GHz. Note that these curves are also averaged from five devices. The corresponding f_T values for different designs are summarized in Table I. For Device B with the gate wiring removed (originally connected to M3), the induced parasitic $C_{\rm gs}$ and $C_{\rm gd}$ are both reduced; therefore, the devices present an improved f_T (~102 GHz, increased by ~15%) compared with that in Device A. With the reduced $C_{\rm total}$ of ~14% for Device B (g_m unchanged), the corresponding f_T improvement estimated by (1) is ~16%, which agrees well with measurements. Moreover, for Device C with the source/drain interconnects further simplified from M4/M2 to M2/M1, the parasitic source resistance is reduced. As a result, the intrinsic transconductance and the dc current increase, and the f_T is further improved to 108 GHz (increased by ~6% compared with Device B). The results indicate that not only the gate wiring but also the source/drain interconnects/vias are important factors for the f_T. Compared with the f_T of

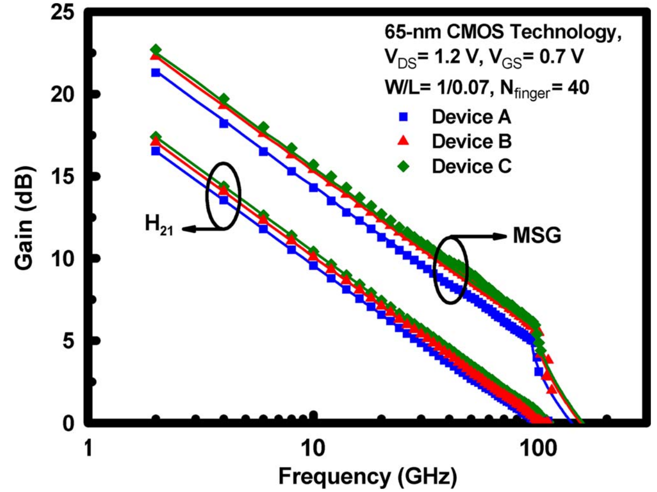

Fig. 2. Short-circuited current gain (H_{21}) and MSG of Devices A, B, and C (at $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = 1.2$ V).

Device A, an improvement of ~21% for Device C can be obtained based on (1), which also agrees well with the measured results.

C. Maximum Oscillation Frequency

Another critical figure of merit for the device RF performance is $f_{\rm max}$. As the gate wiring is simplified from the standard layout (Device A) to that with a ring-type gate (Device B), $f_{\rm max}$ is improved by ~19% (from 130 to 155 GHz). Although Devices B and C have higher R_g, they still present the obviously higher $f_{\rm max}$ than Device A, which can be attributed to the reduced parasitic capacitances in the proposed designs. On the other hand, the better $f_{\rm max}$ of Device C (improved by ~22% than Device A) than Device B can be attributed to the increased intrinsic transconductance and drain current resulting from the further reduced parasitic resistances of the source/drain interconnects/vias. The enhancement of $f_{\rm max}$ estimated by (2) ($g_{\rm ds} \sim 1.5$ mS; f_T, $C_{\rm gd}$, and R_g from Table I)

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are ∼13% and ∼14% for Devices B and C, respectively. As can be seen, the simplified equations predict precisely for the trend of f_T improvement while slightly underestimate that of $f_{\max}$, which could be due to the oversimplified equation and more parameters involved in the calculation with increased discrepancy.

Note that the transistor size selected in our experiments ($1\ \mu\text{m} \times 40$ fingers) has a relatively small width of each finger and a large finger number, which is typically used for RF circuit design owing to the small gate resistance R_g with a better frequency response. In this letter, R_g is no longer the dominant factor for f_T and $f_{\max}$. Instead, the parasitic capacitances and resistances originated from the surrounding interconnect wires play a critical role. Our analysis suggests that the wiring effect should become more pronounced for transistors with increased finger number and reduced width of each finger.

IV. Conclusion

In this letter, the impacts of wiring effect on RF characteristics in 65-nm RF NMOS have been investigated. The proposed design approach demonstrated enhanced RF performance, including both f_T and $f_{\max}$. With a ring-type gate topology and reduced metal interconnect layers, the proposed device layout (Device C) presented significantly improved f_T and $f_{\max}$ up to ∼21% and ∼22%, respectively. Additionally, the device parameters were extracted for quantitative analysis, which showed excellent agreement with the observed trends. This letter provided approaches to reduce the parasitics in advanced MOSFETs and can be applied in standard CMOS process for high-speed circuit design.

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