Edge-extended Design for Improved Flicker Noise Characteristics in 0.13-μm RF NMOS

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Abstract **— This paper proposed a new device layout to improve the flicker noise and generation-recombination (G-R) noise characteristics in 0.13-μm RF N-MOSFETs. By extending the active region edge along the gate, the impact of stress and traps introduced by shallow trench isolation (STI) on device flicker noise was reduced significantly. Under a fixed V_{DS} of 1 V and V_{GS} of 0.5 V, the edge-extended devices (W/L= 1/0.13, N_{finger}= 40) present a reduced noise current spectral density (S_{ID}/I^2) variation to only ~ one third (S_{ID}/I^2 ranges from 4.5×10^{-12} to 9.4×10^{-12} Hz^{-1} at 100 Hz) of that for devices with conventional layout (S_{ID}/I^2 ranges from 2.33×10^{-12} to 1.69×10^{-11} Hz^{-1} at 100 Hz). The associated G-R bulges in flicker noise were almost disappeared with the new design. This study indicates the imperfections and stress at the STI edge are important origins to affect flicker noise characteristics especially for RF devices with a small finger width. In addition, the tradeoff between the improved flicker noise characteristics and the device RF performance is also investigated.**

Index Terms **— Flicker noise, Shallow trench isolation (STI), RF CMOS.**

I. Introduction

The shallow trench isolation (STI) has been developed for advanced CMOS process to improve the isolation between devices with better area efficiency. However, as the device size keeps shrinking down, the stress introduced by STI on the MOSFET characteristics becomes significant. The distance between the edge of STI and the gate has been demonstrated to play a critical role in the device DC characteristics [1]-[3]. The compressive stress caused by STI and stress-control layer on flicker noise in CMOS has also been investigated previously [4]-[5]. Flicker noise of devices is the main limitation to achieve a low phase noise voltage controlled oscillator (VCO) [6]. In many analog/digital and digital/analog converters, the flicker noise also degrades the signal to noise ratio. Studies focused on noise theories and modeling for advanced CMOS technologies were published [7]. T. Oishi *et al.* [8] and H. Lee *et al.* [9] have investigated the influence of various STI structures on silicon-on-insulator (SOI) MOSFETs, which suggested that STI has an obvious effect on device flicker noise characteristics. In addition, the impact of device geometries on flicker and the G-R noise characteristics was discussed in [10]. It has been shown that STI can cause a large variation on the flicker noise level especially for multi-finger RF devices, which is a critical issue for RF circuit applications.

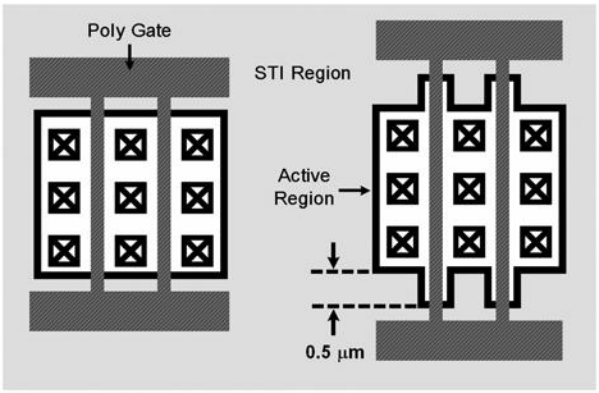

Fig. 1. (a) Conventional layout of RF MOSFETs. (b) layout of RF MOSFETs with an extended active-region of 0.5 μm along the finger.

In this study, we propose a new layout approach to minimize the STI effect on flicker noise characteristics. Many devices of each type from different chips are characterized to obtain a statistical conclusion. The results indicate that STI effect on flicker noise strongly depends on the abrupt transition edge between the STI region and the active area. With the layout proposed here, a clear improvement on the flicker noise variation and the G-R bulges can be observed. Section II describes the devices structure design and the noise measurement setup. Section III presents the experimental results and discussion. Section IV concludes this work.

II. Device Layout Design and Flicker Noise Measurement Setup

Fig. 1 (a) and (b) show the layouts of a conventional multi-finger RF MOSFET and the proposed edge-extended devised, respectively. As can be seen, the proposed new layout in Fig. 1(b) has a 0.5-μm extension of the active region along each side of the finger. For RF design consideration, the devices are typically designed as a multi-finger structure with a relatively small width of each finger to reduce the gate resistance for optimized high-frequency performance. It has been reported that the traps located in the STI edge and the non-uniform stress caused by the STI structure have a great impact on the central channel carriers, which can generate an undesired variation in the flicker noise and DC *I-V*

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characteristics [10]. As shown in Fig. 1, the device active region is surrounded by the STI structure, thus the interface between the STI and the active region exists considerable amount of traps and suffers from a large compressive stress. Such effect is significant for RF devices with a short finger width since the STI edge is close to the main part of the channel for carrier transportation. A simple idea is proposed here as shown in Fig. 1 (b) to alleviate the effect of the STI edge on the device flicker noise characteristics. With the critical transition region farther away from the channel carrier, the stress applied on the carriers can be reduced. In addition, the distance between the traps at the STI edge and the effective channel increases leading to a smaller impact of the traps on the flicker noise characteristics. Devices with two different finger widths including 1 μm and 5 μm, and the corresponding finger numbers of 40, and 8 were designed and tested, which have the same total channel width of 40 μm for a fair comparison.

The measurement setup of flicker noise in this work is similar to that shown in [10]. The measurements were performed on-wafer by employing low-loss RF cables and probes with excellent ground shielding for the signal paths. A low-noise preamplifier with a noise floor of 6.4×10^{-21} V^2/Hz was used to amplify the noise signal. In addition, a battery-powered DC voltage source was used to bias the devices to minimize the additional disturbance from the power supply. Moreover, the devices and the system including the preamplifier and the probe station were enclosed in a shielding box to further reduce the environmental interferences. The noise measurements were performed from 10 Hz to 100 KHz, and the noise floor of the system was well below the noise level of the tested devices in the measured frequency range.

Fig. 2 shows the micrograph of the RF MOSFETs with the ground-signal-ground (G-S-G) RF pads in this study. With well designed pads and the above mentioned system, the device oscillation problem can be effectively avoided to obtain more reliable data. Devices characterized in this study were fabricated by a standard CMOS RF 0.13-μm process, with a threshold voltage of ~ 0.4 V. During the measurements, the gate terminal was AC short-circuited through a large capacitor (~ mF) to obtain the drain noise current spectral density.

III. Results and Discussion

A. Flicker Noise Characteristics

Fig. 3 and Fig. 4 present the normalized drain noise current spectral densities for the conventional RF NMOS devices with W= 1 μm (N_{finger}= 40) and W= 5 μm (N_{finger}= 8), respectively. Data from five devices on different chips are shown in each figure. The gate bias (V_{GS}) varied from 0.5 to 0.8 V under a fixed drain bias (V_{DS}) of 1 V. As can be seen in both Fig. 3

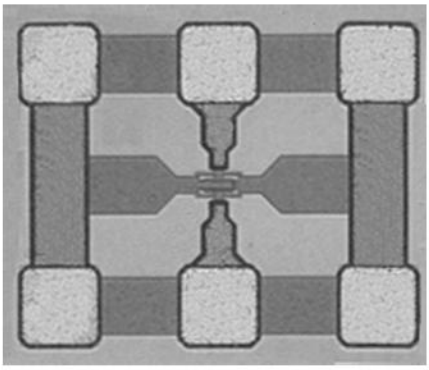

Fig. 2. Test structure of a 0.13 μm RF N-MOSFET with ground-signal-ground RF pads.

and Fig. 4, the devices present a large variation on the noise levels and many G-R noise components are appeared. However, when the edge between STI and the active region is extended as indicated in Fig. 1 (b), a significantly reduced flicker noise variation was observed for the devices with the same width and finger number as shown in Fig. 5 and Fig. 6, respectively. For example, under a fixed V_{DS} of 1 V and V_{GS} of 0.5 V, the edge-extended devices (W/L= 1/0.13, N_{finger}= 40) present a reduced S_{ID}/I^2 variation to only ~ one third (from 4.5×10^{-12} to 9.4×10^{-12} Hz^{-1} at 100 Hz) of that for devices with conventional layout (from 2.33×10^{-12} to 1.69×10^{-11} Hz^{-1} at 100 Hz).

For a deeper understanding, the carrier number fluctuation model is employed to explain the observed trends, which can be described by the following equation [7]:

$$\frac{S_{ID}}{I_{DS}^2}=\left[1+\alpha\mu_{eff}C_{ox}\frac{I_D}{g_m}\right]^2\frac{g_m^2}{I_D^2}\frac{q^2kT\lambda N_t(E_F)}{WLC_{ox}^2}\frac{1}{f} \quad (1)$$

where N_t is the trap density, α is the scattering parameter, μ_{eff} is the effective carrier mobility. In this model, traps are the main origin of flicker noise, while the effective carrier mobility can also affect the noise level. With the conventional layout, the devices suffered non-uniform STI stress especially in the vicinity of the STI edge and the active region, which can cause variations of both carrier mobility and the amount of traps in the channel. As a result, the conventional devices present a large variation of noise current spectral densities (more than one order of magnitude) even under the same bias condition. In the proposed design with the extended edge, the non-uniform stress on the most critical channel area is reduced resulting in a great improvement in the flicker noise characteristics.

In addition, many G-R bulges were observed for conventional devices as shown in Fig. 3 and Fig. 4. However, the proposed devices with the extended edge presented much less G-R bulges as shown in Fig. 5 and Fig. 6, which indicates that G-R noise is strongly related to the traps located on the

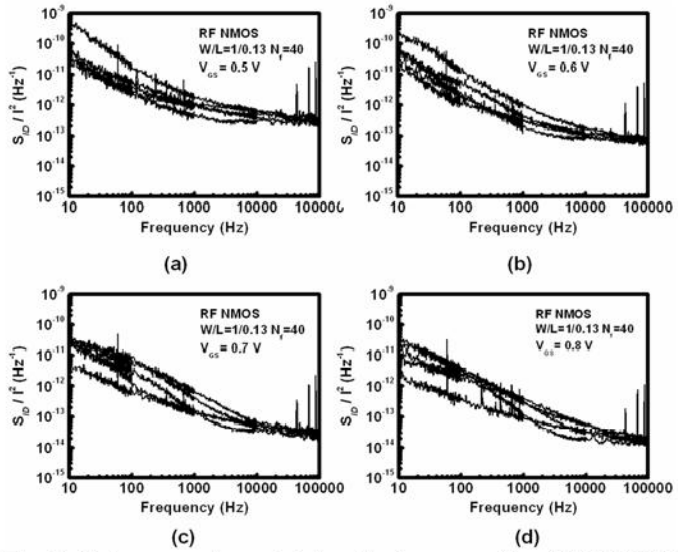

Fig. 3. Noise current spectral density for conventional RF NMOS devices with W= 1 μm and N_{finger}= 40 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

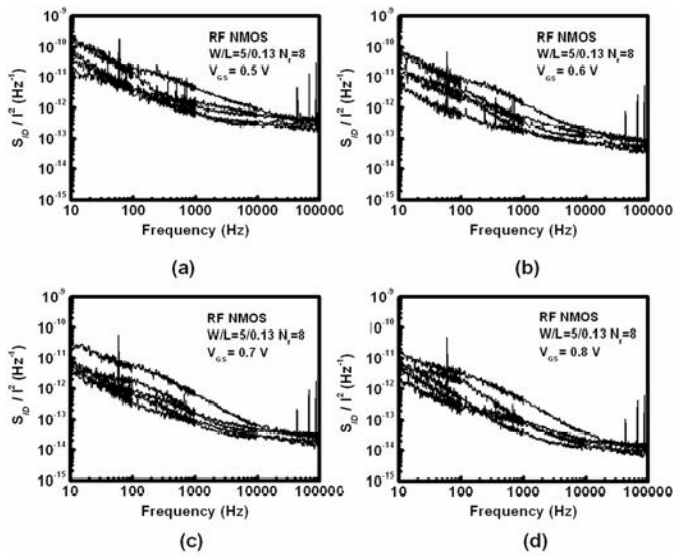

Fig. 4. Noise current spectral density for conventional RF NMOS devices with W= 5 μm and N_{finger}= 8 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

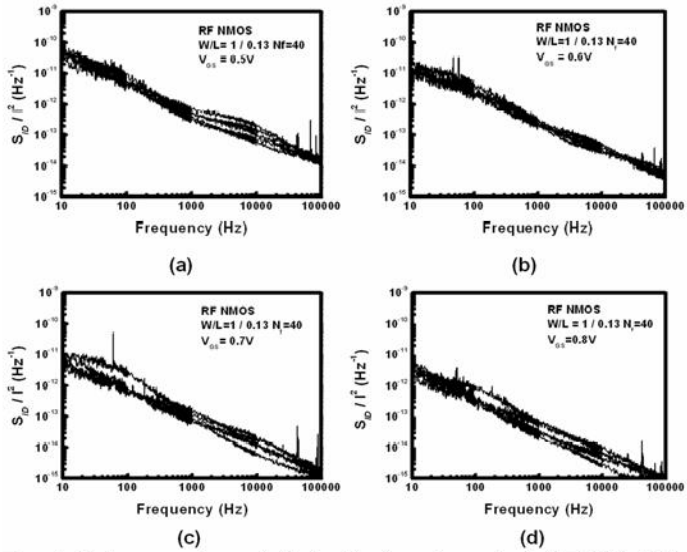

Fig. 5. Noise current spectral density for edge-extended RF NMOS with W= 1 μm, N_{finger}= 40 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

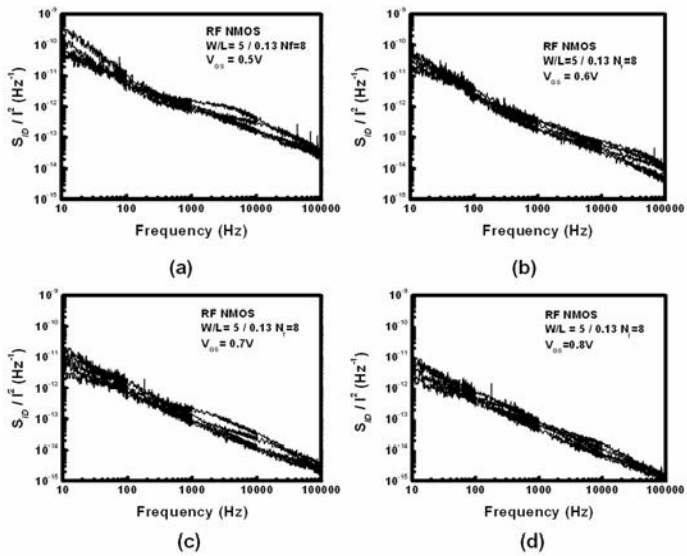

Fig. 6. Noise current spectral density for edge-extended RF NMOS with W= 5 μm, N_{finger}= 8 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

oxide corner of the STI edge. In the conventional design, these traps are closer to the critical channel area. With the new layout approach, the trap-to-channel distance is extended, and the flicker noise of the devices presents a curve close to an ideal 1/*f* characteristic.

B. RF Performance and Parasitic Capacitances

The measured results demonstrated that the proposed design with an extended edge of the active region effectively improved the flicker noise characteristics in RF MOSFETs. It is interesting to further evaluate the additional parasitic capacitances introduced by the extended edges and also the trade-off between the flicker noise characteristics and RF performance. Table I. compares the total capacitances (C_{total}) and the cut-off frequency (f_T) for both types of devices, where the f_T was directly extracted from the measurements, while the C_{total} was estimated based on the simple equation:

$$f_T = \frac{2\pi}{g_m \cdot C_{total}} \tag{2}$$

As shown in Table I, C_{total} increased by ~ 8% for W= 5 μm (N_{finger}= 8) and by ~ 34% for W= 1 μm (N_{finger}= 40) for the edge-extended devices. One may expect that the RF

performance degrades seriously especially for the latter case. As can be seen, the f_T of the device with W= 5 μm (N_{finger}= 8) showed a slight degradation of only ~ 5%, which can be attributed to the increased parasitic capacitances. However, the device with W= 1 μm (N_{finger}= 40) presented an opposite trend to have an improved f_T of ~ 23%. It is obvious that the increased drain current dominates the f_T performance in this case. As shown in Table I, the drain current increases substantially (~ 59%) for W= 1 μm (N_{finger}= 40) devices with edge-extended design. As the edge was extended of each finger, the effective total finger width of the device increased. In addition, the compressive stress applied on the channel carriers is reduced in the new design, thus the stress-induced mobility reduction is smaller leading to an increased drain current. Note that both effects have a higher impact on the devices with a short finger width and more finger numbers. As a result, the W= 5 μm (N_{finger}= 8) devices have a similar f_T for both types of devices, while the W= 1 μm (N_{finger}= 40) devices with edge-extended design has a higher f_T compared to the conventional layout.

TABLE I
COMPARISON OF CONVENTIONAL AND EDGE-EXTENDED RF NMOS DEVICES

	Conventional Devices		Edge-extended Devices	
Bias	V_{DS}= 1 V / V_{GS}= 0.8 V			
W / L	1 / 0.13	5 / 0.13	1 / 0.13	5 / 0.13
N_{finger}	40	8	40	8
C_{total} (fF)	69.5	52.1	93.3	56.5
I_{DS} (mA)	9.5	10.2	15.1	10.7
f_T (GHz)	67.5	90.0	83.0	85.5

As discussed above, despite the additional capacitances introduced by the extended edge along the finger may reduce the f_T, the associated drain current improvement can compensate the effect to achieve a better performance in both RF performance and flicker noise characteristics simultaneously. For flicker noise sensitive blocks in RF applications such as VCOs, the proposed edge-extended layout provides an effective solution to improve the circuit performance.

IV. CONCLUSIONS

In this study, a new device layout for improved flicker noise and G-R noise characteristics in 0.13-μm RF NMOS has been demonstrated. Based on the carrier number fluctuation model, the excellent results can be attributed to less impact from the stress and traps caused by STI in the edge-extended design. The RF performance for the devices has been compared. With additional parasitic capacitances in the proposed design, the devices showed a similar or even higher f_T due to the increased drain current. The proposed edge-extended approach provided an effective solution to minimize the STI effect on flicker and G-R noise characteristics, which can be very useful for the noise sensitive blocks in RF applications.

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