A 79GHz UWB Pulse-Compression Vehicular Radar in 90nm CMOS

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***Abstract*— A 79GHz UWB pulse-compression (PC) vehicular radar system is presented. A PC waveform is a long pulse with internal modulation. The energy of it can be increased without raising the instantaneous peak power. Meanwhile, a PC waveform preserves an equal bandwidth and the range resolution associated with a single pulse waveform. In addition, the PC technique also allows multiple radars operating simultaneously based on the code division multiple accessing (CDMA). In this work, the internal modulation of the PC waveform is binary phase shift keying (BPSK) with a 31-bit length pseudo noise (PN) sequence. The modulation rate is 1 Gb/s and the maximum pulse width is 31 nsec. The CMOS chip presents a self-contained radar system with the transmitter, receiver, frequency synthesizer, and complete timing circuit fully integrated in a standard 90nm CMOS technology.**

***Index Terms*— CMOS, UWB, CDMA, pulse compression, radar, millimeter wave, direct conversion transceiver, pseudo noise code.**

I. Introduction

Fully-integrated silicon-based vehicular radar devices have the potential to offer a low-cost solution for road safety enhancement [1], [2]. In general, radar systems can be classified into continuous wave (CW) and impulse radio (IR) systems. Compared with CW radar systems, IR radar systems have certain advantages in terms of less multi-path effect and higher range resolution. In IR radar systems, the waveform of propagation signal is usually a short pulse which has a large bandwidth but small energy. It results in high range resolution, but low detection probability in a radar system. Although, the overall energy into a decision device in the receiver can be increased through integrating multiple pulses.

A PC waveform (Fig. 1) is a long pulse with internal modulation, it can hold an equal bandwidth and more energy which lead equal range resolution and higher detection probability in comparison with a short pulse. It also allows multiple radars operating simultaneously through the CDMA technique. In this work, a 79GHz CMOS UWB radar employing binary phase-coded PC waveform is reported. With a large instantaneous bandwidth and time-gated operation, a high range resolution within a large detection range can be achieved.

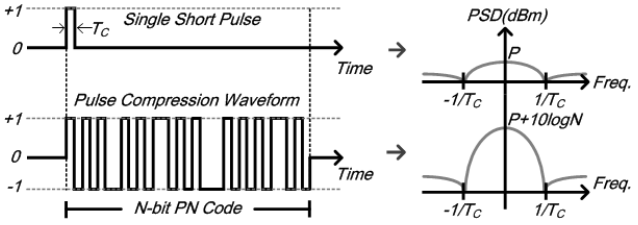

Fig. 1. The waveform and spectrum of a single short pulse and a pulse compression waveform.

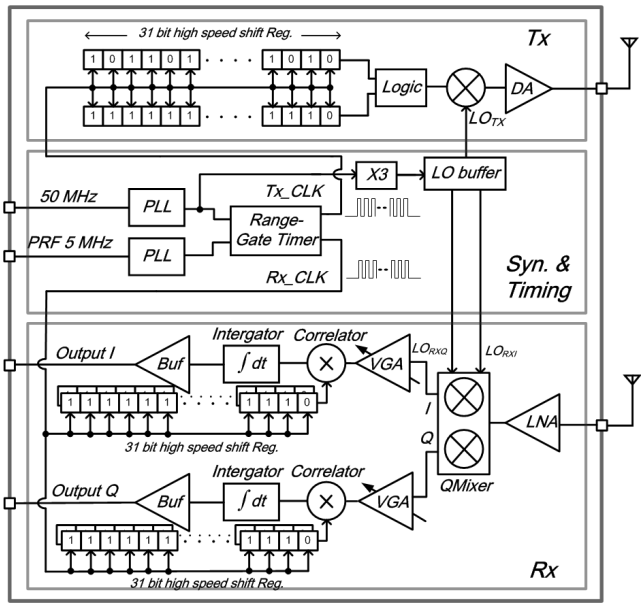

Fig. 2. System-level block diagram of the proposed PC radar system.

II. System Architecture

The proposed CMOS UWB radar architecture is structured as follows (Fig. 2). The transmitting path contains a binary phase coded PC waveform generator, an up-conversion mixer, and a driver amplifier (DA); the receiving path is composed of a low noise amplifier (LNA), quadrature down-conversion mixers, and correlators; a frequency synthesizer generating the mm-wave carrier for frequency up/down-conversion and a timing circuitry discriminating the distance of a target from entire range bins.

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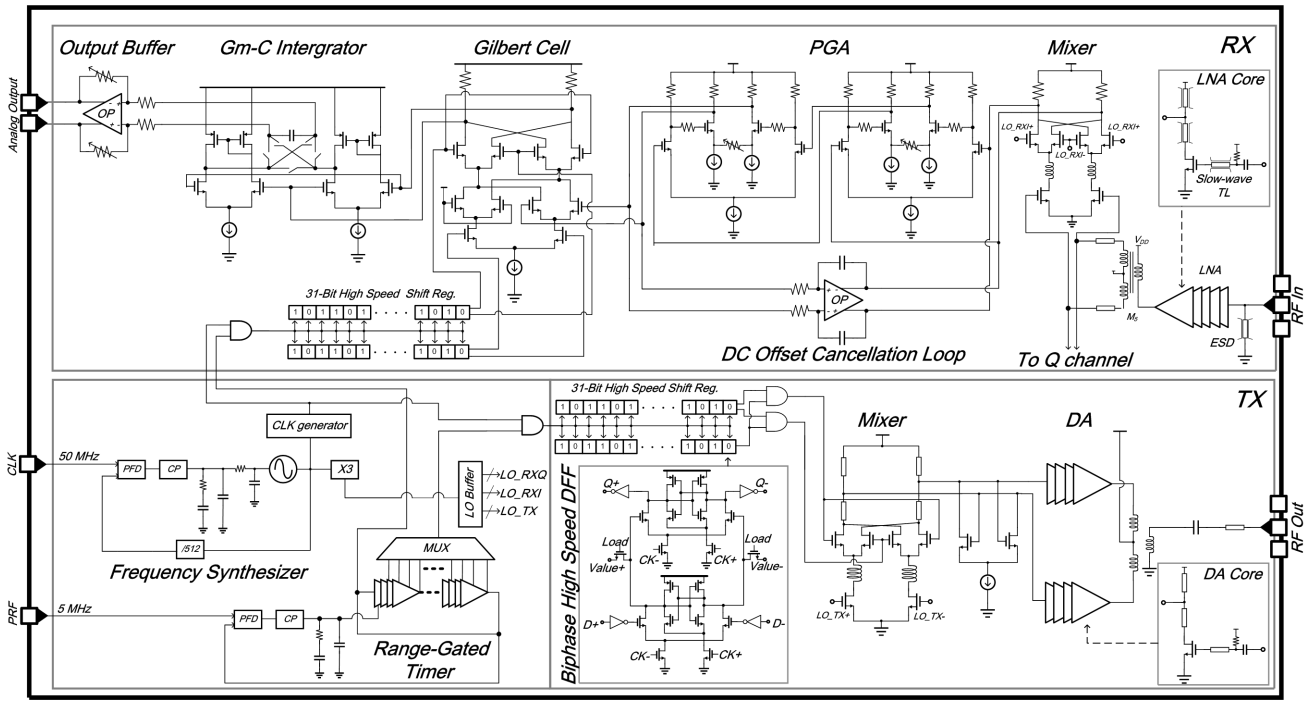

Fig. 3. Simplified PC radar system circuit schematics including transmitter, receiver, frequency synthesizer, and timing circuitry.

In the transmitter, a binary phase-coded PC waveform is generated via a trinary encoder. A trinary code has three levels for signal representation which are positive $(+1)$, negative (-1), and zero (0). It provides binary phase-coded PC waveforms with positive or negative levels inside the pulse interval and zero level outside the pulse interval. The reported trinary encoder comprises two 31-bit parallel differential shift registers with 1GHz clock and a high-speed combinational logic circuitry. One shift register controls the pulse time width and the other sets the binary phase shift keying (BPSK) modulation. The codes for the pulse width and the BPSK modulation are loaded from a series-to-parallel interface. The output digital signals of these two shift registers are fed into a combinational logic circuitry to produce a differential binary phase-coded PC signal in the baseband. The next stage is a mixer which up-converts the baseband pulse to the mm-wave frequency. A DA buffers the waveform generator and delivers pulses to an antenna. The carrier frequency of the mm-wave binary phase coded PC waveform is 79 GHz, the modulation rate is 1 Gb/s in baseband which corresponds to 15cm range resolution, the maximum pulse width is 31 nsec, the pulse repetition frequency is 5 MHz which corresponds to 30m maximum detection range.

In the receiver, the LNA receives and amplifies the pulses which is reflected from a target from antenna. Following the LNA, quadrature mixers down-convert the received signals from the mm-wave band to the base-band. There is a correlator in each quadrature path which functions as a matched filter. It provides high signal-to-noise ratio (SNR) by corrupting the received noise and interferences through cross correlating received signal with a template. The correlator consists of a programmable gain amplifier (PGA), a multiplier, a resettable integrator, and an analog output buffer. The quadrature amplitude of the baseband signals are adjusted by the PGAs based on the programmable length of transmitting codes and the distance of a target to enhance the dynamic range of the receiver. The output signal of each PGA is multiplied with the code template in a current-commutating mixer and the resulting signal is poured into an integrating capacitor. The codes of the template for the pulse width and the BPSK modulation are stored in two parallel high speed shift registers.

A 79GHz frequency synthesizer is implemented to generate the mm-wave carrier signal for both transmitter and receiver. A range-gated timer which measures time of flight (TOF) of pulses It provides 400 range bins within the maximum detection range of 30 m.

III. Circuit Schematics

The simplified circuit schematics of the reported radar system are shown in Fig. 3.

The transmitter starts with a trinary encoder which produces differential modulated signal in baseband. Fully-customized high-speed biphase flip flops are realized in

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TABLE I

SUMMARY AND COMPARISON

	This Work	[2]
Technology	CMOS 90 nm	SiGe 0.18 um
Frequency	75-80 GHz	22-29, 76-81 GHz
Tx Output Power	-17 dBm	10.5 dBm*
Feature	Pulse Compression	Single Pulse
Code Length	31 bit	N/A
PC Technique	BPSK	N/A
Conversion Gain	10 dB†	31 dB*
DSB NF	9 dB†	8 dB*
Input P1dB	-16 dBm†	-30.7 dBm*
Phase Noise @ 1 MHz	-78 dBc/Hz	-100.4 dBc/Hz*
Supply Voltage	1.5 V	2.5/1.8 V
Power	1.37 W	0.61 W*
Die Area	4.31 mm²‡	7.4 mm²

* Only the performance of 76-81GHz band is shown

† Only the performance of LNA and frequency down-converter

‡ Active area

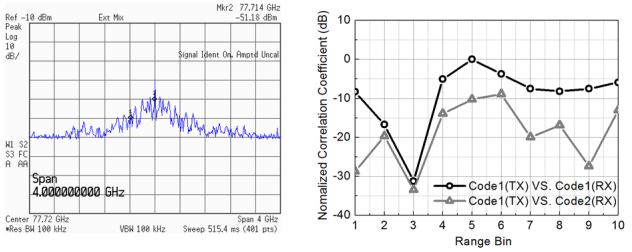

Fig. 4. (a) The spread spectrum of a PC waveform. (b) The loopback measurement results.

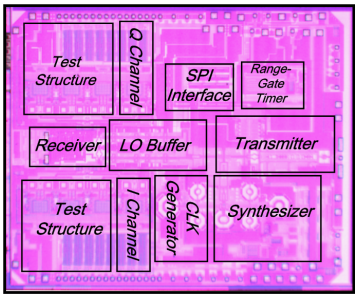

Fig. 5. Chip microphotograph of the mm-wave PC radar system.

the shift register of the trinary encoder. The double balanced current-commutating Gilbert cell is implemented for the frequency up-converter to minimize the LO-to-RF feedthrough.

The LNA is a five-stage single-ended common-source amplifier with slow-wave transmission-line matching networks. The input matching network is accomplished by using shunt and series inductors. The shunt inductor acts as an electrostatic discharge (ESD) protection device. The frequency down-converters utilize a similar design as the frequency up-converter. The PGA is a two-stage Cherry-Hooper amplifier with a local feedback to increase its bandwidth. An analog correlator is implemented to achieve high-speed and wide-bandwidth operation. The correlator in each quadrature path includes a current-commutating mixer, a Gm-C integrator, and an analog output buffer.

The carrier of the PC waveforms is generated by an integer-N phase locked loop (PLL) and a frequency tripler. The range-gated timer is mainly composed of a ring-oscillator-based PLL and a multiplexer.

IV. MEASUREMENT RESULTS

Table I summarizes the measured performance of the reported CMOS UWB PC radar chip and compares it with the work reported in [2]. The transmitted spread spectrum of a binary phase-coded PC waveform with a 2GHz bandwidth and 77GHz carrier frequency is shown in Fig. 4(a). The modulation rate is 1 Gb/s in baseband, the code length of PN code is 31, and the pulse width is 31 nsec. The loopback measurement results are shown in Fig. 4(b). The transmitter is serially connected to the receiver through RF cables. By changing the transmitted timing of the PC signals with a step of 500 psec, the receiver can sense the loop-back signal at different range bins. The black and gray curves represent the correlation coefficients versus range bins when the transmitted signal is identical and different to the template of receiver, respectively. It shows that the reported PC radar can search range bins through time-gated mechanism and corrupt interferences from other users. The chip microphotograph is shown in Fig. 5.

V. CONCLUSION

A 79GHz single-chip PC radar in a 90nm CMOS technology has been demonstrated. PC radars are immune to multi-path effect and can achieve high range resolution simultaneously. Therefore, it is a promising candidate for vehicular radar applications.

VI. ACKNOWLEDGMENT

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