Design and Characterization of a CMOS Micromachined Capacitive Acoustic Sensor

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Abstract— **This work presents a CMOS micromachined capacitive sensor for detection of acoustic pressure transmitted through the air. The post micromachining steps performed at chip level start with a sacrificial metal etch, followed by a dielectric reactive ion etch. The fabricated device has a suspended plate of 65 μm in diameter with four support beams, producing an initial sensing capacitance of 35 fF. The suspended plate has a resonant frequency of 1.3 MHz. The measured input-referred circuit noise is 0.35 $\mu V/Hz^{1/2}$. The measured sensor output is 3.5 μV at an electrode bias of 10 V, which is equivalent to a capacitance change of 2.9×10^{-2} aF and a displacement of 0.31 pm. The corresponding acoustic force and pressure acting on the sensor are 0.33 nN and 0.075 Pa, respectively.**

I. Introduction

Ultrasound is used in a wide variety of applications, most notably in medical imaging [1] and nondestructive evaluation [2]. The research on capacitive micromachined ultrasonic transducers has been increasingly popular over the past ten years, as they are capable of providing lower mechanical impedances and a better impedance matching to the fluid medium than those of the conventional bulk piezoelectric transducers. The electro-mechanical coupling behaviors in air [3] and fluid [4] have both been studied in prior published work. The membrane-type transducers with uniform quality can be batch fabricated at low cost by the similar processes for making integrated circuits.

From the signal-processing standpoint, it is desirable to achieve monolithic integration of the signal-conditioning circuits such that the tasks for routing and multiplexing of arrayed signals can be conveniently achieved on a single chip. Prior work has reported transducers combining electrothermal actuation and piezoresistive sensing [5], and electrostatic actuation and capacitive sensing [6]. Rufer [5] reported thermally-actuated dielectric membranes fabricated by a backside silicon etch in a 0.8-μm CMOS process. By using an intermediate CMOS micromachining process, polysilicon membranes [6] were fabricated by using silicon dioxide as the sacrificial material for structural release. The integration of sensing electronics for capacitive detection is especially beneficial for promoting the measured signal-to-noise ratio. The reason is that the sensing capacitance produced by a released membrane could be in the order of tenths to hundreds of fF. The value is much less than the parasitic capacitances contributed largely from wire bonding in a two-chip solution, which normally results in a reduced signal-to-noise ratio. The advantage of integration is well evidenced by the success of many highly-sensitive capacitive inertia sensors [7].

This paper focuses on exploring the sensing capabilities of an air-coupled capacitive ultrasonic sensor fabricated in a conventional CMOS process. Prior published work has generally concerned the 1-D or 2-D capacitive sensing arrays in which the signal-to-noise ratio is promoted by connecting multiple sensing elements in parallel to form a large sensing capacitance. This work will examine the issues of sensitivity and resolution of individual sensing element, as they have been less discussed in related literatures. Different from the intermediate CMOS micromachining process adopted in [6], our devices are fabricated after CMOS completion at the die level, such that the CMOS foundry does not need to alter the existing processing steps.

II. Device Fabrication

The TSMC 0.35-μm two-polysilicon four-metal (2P4M) CMOS process is used for sensor fabrication. The process flow in Fig. 1 shows the development of a released microstructure in cross-section. After completion of the CMOS foundry process, most of the die area, including the bond pads, is covered by the top passivation layer except for the openings beside the structure for release etch. As shown in Fig. 1(b), we perform a sacrificial wet etch of stacked metal (aluminum) and via (tungsten) layers through the openings by using a mixed H_2SO_4/H_2O_2 etchant, with the dielectric layers for etch protection. The solution is constantly heated at 85°C, while H_2O_2 is replenished regularly to maintain the etching rate. The top and bottom electrodes for capacitive sensing are formed when the sacrificial metal-3 layer is removed. To avoid stiction due to liquid remaining between the movable and fixed electrodes, the die is immersed in isopropyl alcohol (IPA) for 30 minutes, followed by a hotplate bake at 90°C for five minutes. Then a reactive ion etch using the CHF_3/O_2 plasma (100 sccm: 5 sccm) removes the passivation remaining on top of the structure and bond pads (Fig. 1(c)). According to the processing steps, the shape of the suspended microstructure is defined by the passivation openings. The use of large-size vias

for the sacrificial metal etch is against foundry design rules but acceptable for fabrication. The separation between the suspended plate and the bottom is about 0.64 µm of the metal-3. The etching rates of tungsten via and aluminum layer are found to be around 0.04 µm/min. and 1.5 µm/min., respectively.

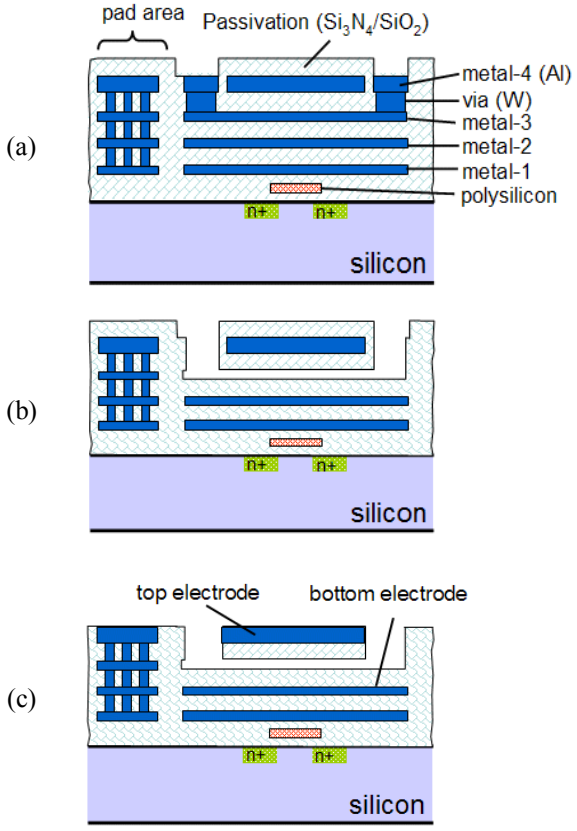

Figure 1. Post-CMOS micromachining steps: (a) after completion of CMOS, (b) sacrificial metal etch for structural release, and (c) removal of the top passivation layer.

III. DESIGN

The released microstructure shown in Fig. 2 is doubly clamped with four support beams connected to anchors. The circular plate is 65 µm in diameter and the support beams are 20 µm in both width and length. The suspended structure consists of one metal and one dielectric layers, producing a total thickness of about 1.9 µm.

The out-of-plane spring constant of the suspended structure is an important parameter for calculating the measured sensitivity in terms of the applied acoustic pressure. The result from finite-element simulation shows a spring constant of 1070 N/m. The Young's modulus of aluminum and silicon dioxide used in the simulation are 70 GPa and 75 GPa, and the film stresses are set to zero due to the lack of data from the CMOS foundry. Tensile and compressive stresses tend to increase and decrease the stiffness, respectively. For our case the overall effect is unclear with the composition of a tensile metal layer and a compressive silicon dioxide layer.

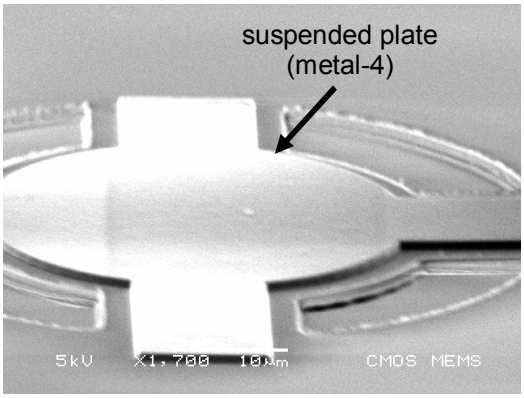

Figure 2. Scanning electron micrograph of the released microstructure.

The top and bottom sensing electrodes are the metal-4 and metal-2 layers in the 2P4M CMOS process. The capacitor consists of an air gap and two dielectric layers on the electrodes. The initial sensing capacitance is expressed as:

$$C_{s0} = \frac{\varepsilon_0 A}{(h_1 + h_2)\frac{\varepsilon_0}{\varepsilon_s} + x_0} = \frac{\varepsilon_0 A}{g_0} \qquad (1)$$

where ε_0 is the permittivity of air, ε_s is the permittivity of silicon dioxide, A is the electrode area, h_i is the dielectric thickness, and x_0 is the initial air gap. The initial sensing capacitance is 35 fF by calculation.

The sensing circuit as shown schematically in Fig. 3 contains two p-channel source followers to provide a voltage gain close to one. The resulting circuit area is small such that it can be placed directly beneath the sensor. The use of PMOS input transistors helps to reduce the flicker noise at low frequencies. The first source follower uses a small-size input transistor for the purpose of providing a small input capacitance with the value comparable to that of the sensing capacitance C_{s0}. The d.c. path at the circuit input is provided by the transistor operated in the subthreshold region. The second source follower with a larger input transistor is used for driving the output pad. For signal detection, a d.c. voltage is applied at the top electrode of the sensing capacitor to produce the displacement current, $i_s = V_{dc}\, dC_s / dt$. The sensing capacitance is $C_s(t) = C_{s0} + C_{s0}(x/g_0)\sin(\omega_a t)$,

where x is the displacement and ω_a is the acoustic frequency. The displacement current, after flowing into the input capacitance C_{in} of the pre-amp, produces the sensed voltage given by:

$$v_o = \frac{x}{g_0}\frac{C_{s0}}{C_{in}}V_{dc} \tag{2}$$

For example, the sensed voltage is 38 μV when x is 0.01 nm, g is 2.6 μm, V_{dc} is 10 V, and the value of C_{s0} is equal to that of C_{in}.

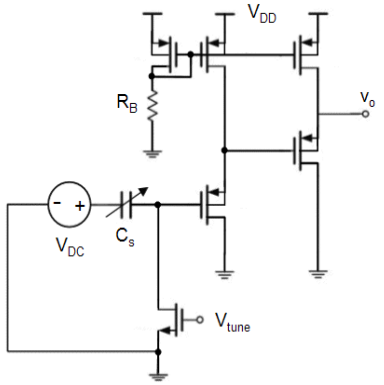

Figure 3. Schematic of the sensing pre-amp.

Large transistors are commonly used in conventional low-noise circuit design for reducing the transistor thermal noise and flicker noise. Large input transistors, however, also reduces the sensed signal owing to the increase of the gate capacitance. When the flicker noise is considered for signal-to-noise optimization, it was suggested that the gate capacitance value of the transistor should be equal or smaller than the total of the sensing and the interconnect capacitances [7]. To our advantage, the sensing circuit can be placed underneath the sensor to get a minimum interconnect capacitance. The sensing circuit has a total area of 130 μm by 40 μm.

IV. Experiment

The frequency response of the sensing circuit was measured by an Agilent 4395A network analyzer. Fig. 4 shows a measured gain of about -7.5 dB, giving a measured C_{in} of 48 fF with a simulated C_s of 35 fF. The value is comparable to the sensing capacitance such that a good signal-to-noise ratio can be obtained. The subthreshold transistor in front of the sensing circuit provides the required dc path, and the accompanied high-pass filtering characteristic is adjusted by its gate-to-source voltage. The equivalent resistance value provided by the subthreshold transistor is more than GΩ at low V_{GS} values.

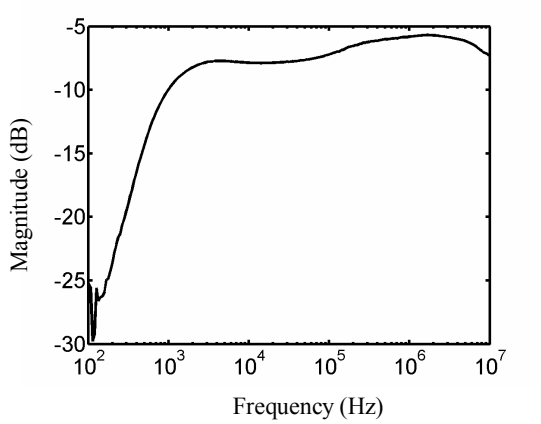

Figure 4. Frequency response of the sensing pre-amp.

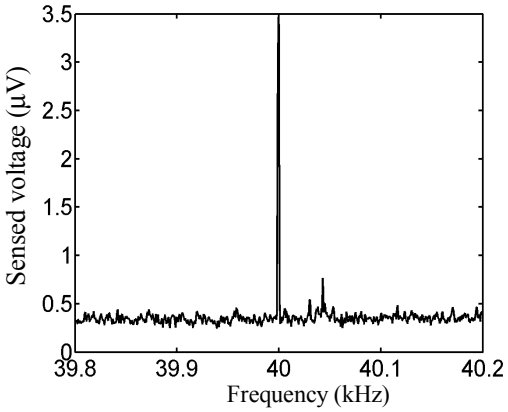

Figure 5. Measured spectrum of the sensed signal at 40 kHz.

For electromechanical characterization, a 40-kHz acoustic emitter driven by a function generator was placed face-to-face with respect to the sensor chip at a distance of about 1 cm. By applying 10 V (V_{DC}) on the top electrode of the sensing capacitor C_s, the output spectrum was measured at a resolution bandwidth of 1 Hz as shown in Fig. 5. The peak value at 40 kHz is 3.5 μV and the noise floor is 0.35 $\mu V/Hz^{1/2}$. Fig. 6 shows the sensor output by gradually increasing the dc voltage on the electrode to 150 V. The value increases accordingly due to the increased displacement current. HSpice simulation was used for calculation of the corresponding capacitance changes. The measured value of 3.5 μV at 10 V is equivalent to a capacitance change of 2.9×10^{-2} aF and a displacement of 0.31 pm based on assumption of a parallel-plate capacitor. The corresponding force and pressure applied on the suspended plate can be calculated by using the simulated spring constant of 1070 N/m, and the values are 0.33 nN and 0.075 Pa, respectively.

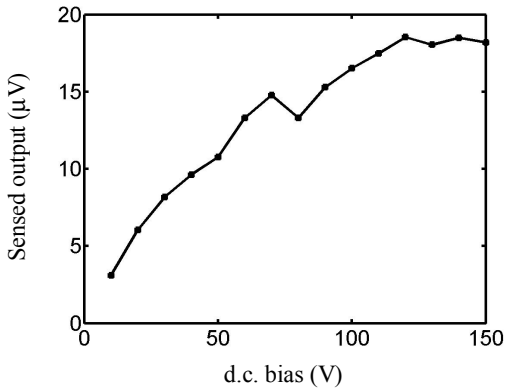

Figure 6. Relationship of the measured sensor output with respect to the d.c. bias on the sensing capacitor.

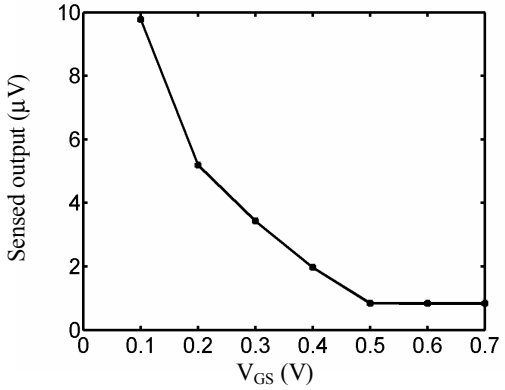

Figure 7. Measured sensor output with respect to the source-to-drain voltage of the subthreshold transistor.

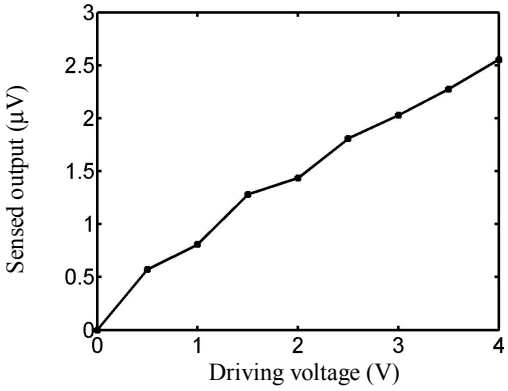

Figure 8. Relationship of the sensor output and the emitter driving voltage.

By increasing the V_{GS} value of the subthreshold transistor to reduce its resistance, the total impedance at the circuit input decreases accordingly and results in reduction of the sensor output. Fig. 7 shows that the output decreases from 9.8 μV to 0.9 μV for V_{GS} values of 0.1 V and 0.7 V, respectively. Fig. 8 shows the linear increase of the sensor output with respect to the driving voltage of the acoustic emitter.

V. Conclusion

In this paper, we have proposed a convenient post-CMOS micromachining process for making capacitive ultrasonic sensors at die level. The suspended microstructure with a high stiffness in the out-of-plane direction can be successfully released without stiction during the wet etch. The sensing electrodes are separated by a sub-μm air gap defined by the sacrificial metal layer. The dielectric layers on electrodes prevent electrical breakdown when a high d.c. voltage is applied across the electrodes for capacitive sensing. Monolithic integration of the sensing circuit greatly reduces the parasitic effect which would otherwise negatively impact the measured signal-to-noise ratio, allowing capacitive detection of less than 10^{-18} F.

Acknowledgment

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