A Necessary and Sufficient Condition for SDL Constructions of Optical FIFO Queues

Jay Cheng, Hsin-Hung Chou, and Chih-Heng Cheng

Abstract

Recently, constructing optical queues by using optical crossbar Switches and fiber Delay Lines (SDL) has been recognized as a key research issue for all-optical packet switching. In this paper, we focus on SDL constructions of optical FIFO queues. We consider a network element consisting of a $1 \times 2$ optical crossbar switch, $2k + 1$ $2 \times 2$ optical crossbar switches, and $2k + 1$ fiber delay lines of lengths $\ell_0, \ell_1, \ldots, \ell_{2k}$. Assume that $\ell_{k-1}^k = (\ell_0, \ell_1, \ldots, \ell_{k-1}) \in A_k$, where $A_k$ is the set of all sequences of fiber delays so that any nonnegative integer $x$ with $0 \leq x \leq \sum_{j=0}^{k-1} \ell_j$ has a unique representation by the $C$-transform of $x$ with respect to $\ell_{k-1}^k$. The main contribution of this paper is to provide an explicit control scheme that explicitly specifies the connection patterns of the optical crossbar switches, and obtain a necessary and sufficient condition on the lengths $\ell_k, \ell_{k+1}, \ldots, \ell_{2k}$ (specifically, the condition in (A1) in Section I) for such a network element to be operated as an optical FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ under our proposed control scheme. The key idea in our proposed control scheme is to operate the network element such that packets stored in the network element satisfy an ordered property and a circularly contiguous property, which lead to the properties required of a FIFO queue.

Index Terms

FIFO queues, optical buffers, optical queues, optical switches, switched delay lines (SDLs).

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I. INTRODUCTION

One of the key bottlenecks toward all-optical packet-switched networks is the lack of optical buffers for conflict resolutions among packets competing for the same resources. As optical packets cannot be easily stopped, stored, and forwarded, currently such conflicts are resolved by first converting optical packets into electronic packets, storing them in electronic buffers, and then converting electronic packets back into optical packets. However, both the O-E conversions and the E-O conversions incur tremendous overheads, and hence the transmission speed advantage of photons over electrons cannot be fully exploited in current packet-switched networks. As the demand for transmission speed/bandwidth in high-speed packet-switched networks is ever increasing, constructions of optical buffers has been well recognized as one of the most critically sought after optical technologies in all-optical packet-switched networks.

Currently the only known way to "store" optical packets without converting them into other media is to direct them via optical crossbar switches through fiber delay lines. The idea is to route optical packets to the right place at the right time so as to achieve exact emulations of the desired optical buffers. As such, constructing optical buffers directly via optical crossbar Switches and fiber Delay Lines (SDL) has received a lot of attentions recently in the literature [1]–[48]. Specifically, theoretical studies on the constructions of many types of optical queues have been reported, including output-buffered switches in [5]–[10], first-in-first-out (FIFO) multiplexers in [5] and [10]–[20], FIFO queues in [20]–[25], last-in-first-out (LIFO) queues in [22], [23], and [26], priority queues in [27]–[31], time slot interchanges in [20] and [32], linear compressors, linear decompressors, non-overtaking delay lines, and flexible delay lines in [20] and [33]–[38], FIFO contractors, LIFO contractors, and absolute contractors in [39]. Furthermore, results on the fundamental complexity of SDL constructions of optical queues can be found in [40] and performance analysis for optical queues has been addressed in [41]–[42]. For review articles on SDL constructions of optical queues, we refer to [43]–[48] and the references therein.

![Diagram](image)

**Fig. 1.** The network element for the construction of an optical FIFO queue with buffer $\sum_{j=0}^{2k} \ell_j$.

In this paper, we focus on SDL constructions of optical FIFO queues which are commonly used
in everyone’s daily life. FIFO queues are often used in different types of switch architectures, such as the output queues in output-buffered switches [49], the virtual output queues in input-buffered switches [50], and the central buffers in load-balanced Birkhoff-von Neumann switches [51]. Among the constructions of optical FIFO queues in the literature [20]–[25], the constructions in [21] and [24] are the most efficient in terms of the required number of $2 \times 2$ optical crossbar switches. Specifically, it was shown in [21] and [24] that an optical FIFO queue with buffer $b = 2^{k+1} - 1$ can be constructed by using a $1 \times 2$ optical crossbar switch, $2k+1$ $2 \times 2$ optical crossbar switches, and $2k+1$ fiber delay lines as shown in Figure 1, where the lengths of the $2k+1$ fiber delay lines are given by $l_0 = l_{2k} = 2^0, l_1 = l_{2k-1} = 2^1, \ldots, l_{k-1} = l_{k+1} = 2^{k-1}, l_k = 2^k$. In other words, approximately $2 \log B 2 \times 2$ optical crossbar switches are needed to construct an optical FIFO queue with buffer $B$.

In [21], a three-stage SDL construction was proposed and the three-stage construction was then recursively expanded for the construction of an optical FIFO queue with buffer $2^{k+1} - 1$ as shown in Figure 1. The main idea in [21] is to operate the three-stage construction according to the joining-the-shortest-queue and serving-the-longest-queue policy. However, to completely determine the connection patterns of the optical crossbar switches, one needs to keep track of the corresponding longest queue and shortest queue at each recursion, and this becomes very complicated and cumbersome when the number of recursions becomes large. In [24], a packet scheduling algorithm was proposed so that arrival packets are temporarily buffered in the first $k$ fiber delay lines in Figure 1 before they can be routed to the last $k+1$ fiber delay lines and stored consecutively in the last $k+1$ fiber delay lines in a back-to-back manner. However, there is no explicit control scheme available in [24] to completely determine the connection patterns of the optical crossbar switches. Such a problem proves to be very difficult and challenging, and so far there are no known results on determining the connection patterns of the optical crossbar switches in Figure 1.

In this paper, we also consider the network element in Figure 1. We assume that $l_{0}^{k-1} = (l_0, l_1, \ldots, l_{k-1}) \in A_k$, where $A_k$ is given by

$$A_k = \left\{ \begin{array}{cccc} b_{0}^{k-1} & \in & (Z^+)^k : & l_0 = 1 \text{ and } 1 \leq l_i \leq \sum_{j=0}^{i-1} l_j + 1, \text{ for } 1 \leq i \leq k - 1 \end{array} \right\}. \quad (1)$$

We note that it is shown in [14] that $A_k$ is the set of all sequences of fiber delays so that any nonnegative integer $x$ with $0 \leq x \leq \sum_{j=0}^{k-1} l_j$ has a unique representation by the $C$-transform of $x$ with respect to $l_0^{k-1}$. Furthermore, we consider a much more general condition on the lengths $l_k, l_{k+1}, \ldots, l_{2k}$ of the $k+1$ fiber delay lines such that they satisfy the condition in (A1) below.

$$(A1) \quad l_k \leq \sum_{j=0}^{k-1} l_j + 1, \quad (2)$$
\[ \ell_{2k} = 1 \text{ and } 1 \leq \ell_i \leq \sum_{j=i+1}^{2k} \ell_j + 1, \text{ for } k \leq i \leq 2k - 1, \]  
\[ \ell_i \mod \ell_{i+1} = 0, \text{ for } k \leq i \leq 2k - 1. \]  

The main contribution of this paper is to provide an explicit control scheme that explicitly specifies the connection patterns of the \(1 \times 2\) optical crossbar switch and the \(2k+1 \times 2\) optical crossbar switches in the network element in Figure 1, and show that the condition in (A1) is a necessary and sufficient condition on the lengths \(\ell_k, \ell_{k+1}, \ldots, \ell_{2k}\) for such a network element to be operated as an optical FIFO queue with buffer \(\sum_{j=k}^{2k} \ell_j\) under our proposed control scheme. Such an explicit control scheme is very simple as it only requires one to keep track of the number of packets in each fiber delay line, the positions of the earliest arrival packet and the latest arrival packet in each nonempty fiber delay line, and whether there is a packet at the lower output link of the \(k\)th \(2 \times 2\) optical crossbar switch. Therefore, in our constructions we not only provide an explicit control scheme, but also allow more general choices of the lengths of the fiber delay lines in Figure 1.

This rest of this paper is organized as follows. In Section II, we state the basic assumptions in this paper and recall the definition of a FIFO queue in [21]. In Section III, we describe the proposed explicit control scheme and show that the condition in (A1) is a necessary and sufficient condition for the network element in Figure 1 to be operated as an optical FIFO queue under our proposed control scheme. Finally, a brief conclusion is made in Section IV.

II. Preliminaries

In this paper, we make the following basic assumptions that are usually adopted in the SDL literature: (i) Packets are of the same size (we note that for variable-length bursts, they can be first segmented into fixed-size packets at the sources and then reassembled at the destinations). (ii) Time is slotted and synchronized so that a packet can be transmitted within a time slot. (iii) A \(2 \times 2\) crossbar switch is a network element with two input links and two output links that realizes the two permutations between its inputs and its outputs. (iv) A fiber delay line of length \(\ell\) is an optical link that requires \(\ell\) time slots for a packet to traverse through.

We now recall the definition of a (discrete-time) FIFO queue in [21].

![FIFO queue](image)
Definition 1 (FIFO queues) A FIFO queue with buffer $B$ is a network element with one input link, two output links, and one control input (see Figure 2). The input link is for arrival packets, one output link is for departure packets, and the other output link is for loss packets. Let $c(t) \in \{0, 1\}$ be the state of the control input at time $t$. We say that the FIFO queue is enabled at time $t$ if $c(t) = 1$, and is disabled at time $t$ if $c(t) = 0$. Also, let $a(t) \in \{0, 1\}$ be the number of arrival packets from the arrival link at time $t$, $d(t) \in \{0, 1\}$ be the number of departure packets through the departure link at time $t$, $\ell(t) \in \{0, 1\}$ be the number of loss packets dropped through the loss link at time $t$, and $q(t) \in \{0, 1, \ldots, B\}$ be the number of packets stored in the buffer at time $t$ (at the end of the $t$th time slot). Then a FIFO queue with buffer $B$ satisfies the following four properties.

(P1) Flow conservation: Packets from the arrival link are either stored in the buffer or transmitted through the two output links. Therefore, we have

$$q(t) = q(t - 1) + a(t) - d(t) - \ell(t).$$

(P2) Nonidling: If the control input is enabled at time $t$, i.e., $c(t) = 1$, then there is always a departure packet when there are packets in the queue at time $t$ (which consist of the packets stored in the buffer at time $t - 1$ and the arrival packet from the arrival link at time $t$). Otherwise, there is no departure packet at time $t$. Therefore, we have

$$d(t) = \begin{cases} 1, & \text{if } c(t) = 1 \text{ and } q(t - 1) + a(t) > 0, \\ 0, & \text{otherwise}. \end{cases}$$

(P3) Maximum buffer usage: If the control input is disabled at time $t$, i.e., $c(t) = 0$, then an arrival packet is lost only when the buffer is overflowed once it is admitted into the queue at time $t$. Otherwise, there is no loss packet at time $t$. Therefore, we have

$$\ell(t) = \begin{cases} 1, & \text{if } c(t) = 0, q(t - 1) = B, \text{ and } a(t) = 1, \\ 0, & \text{otherwise}. \end{cases}$$

(P4) FIFO departure: If there is a departure packet at time $t$, i.e., $d(t) = 1$, then the departure packet at time $t$ is the earliest arrival packet among all of the packets in the queue at time $t$ (which consist of the packets stored in the buffer at time $t - 1$ and the arrival packet from the arrival link at time $t$).

III. THE PROPOSED EXPLICIT CONTROL SCHEME AND THE MAIN THEOREM

In this paper, we view the network element in Figure 1 as a concatenation of a $1 \times 2$ optical crossbar switch and $2k + 1$ cells, where each cell consists of a $2 \times 2$ optical crossbar switch and one fiber delay line that is connected from the upper output link of the $2 \times 2$ optical crossbar switch back to its upper input link. Call the $2k + 1$ cells in Figure 1 cell 0, cell 1, \ldots, cell $2k$ (from left to right), and call the $2k + 1 2 \times 2$ optical crossbar switches in these cells switch 0, switch 1, \ldots, switch $2k$ (from left to right).
For ease of presentation, we call the lower input link (resp., lower output link) of switch \( i \) the input link (resp., output link) of cell \( i \) for \( i = 0, 1, \ldots, 2k \). From Figure 1, we can see that the input link of the \( 1 \times 2 \) optical crossbar switch is connected to the arrival link of the FIFO queue, its upper output link is connected to the input link of cell 0, and its lower output link is connected to the loss link of the FIFO queue. Furthermore, the output link of cell \( i \) is connected to the input link of cell \( i + 1 \) for \( i = 0, 1, \ldots, 2k - 1 \), and the output link of cell \( 2k \) is connected to the departure link of the FIFO queue. Let \( a_i(t) \in \{0, 1\} \) be the number of packets at the input link of cell \( i \) at time \( t \) and \( d_i(t) \in \{0, 1\} \) be the number of packets at the output link of cell \( i \) at time \( t \) for \( i = 0, 1, \ldots, 2k \). Then we immediately see that \( d_i(t) = a_{i+1}(t) \) for \( i = 0, 1, \ldots, 2k - 1 \), and \( d_{2k}(t) = d(t) \) for all \( t \).

As in [21], the \( 1 \times 2 \) optical crossbar switch in Figure 1 is used for admission control so that the maximum buffer usage property in (P3) is satisfied. Specifically, an arrival packet from the arrival link of the FIFO queue is admitted into the FIFO queue (by connecting the input link of the \( 1 \times 2 \) optical crossbar switch to its upper output link so that the arrival packet is routed to the input link of cell 0) only when the buffer of the FIFO queue is not overflowed after the admission of the arrival packet; otherwise, the arrival packet is dropped through the loss link (by connecting the input link of the \( 1 \times 2 \) optical crossbar switch to its lower output link so that the arrival packet is routed to the loss link of the FIFO queue).

In this paper, we assume that the network element in Figure 1 is started from an empty system at time 0, and we label packets admitted into the network element from 1, 2, \ldots according to their arrival times (from the earliest arrival packet to the latest arrival packet) so that an earlier arrival packet has a smaller label than that of a later arrival packet. Furthermore, we say that a \( 2 \times 2 \) optical crossbar switch is set to the “cross” (resp., “bar”) state at time \( t \) if its upper input link is connected to its lower (resp., upper) output link and its lower input link is connected to its upper (resp., lower) output link during the \( t \)th time slot. We assume for simplicity that the time to set up the connection patterns of the switches in Figure 1 and the time to route packets through the switches and their input links and output links are negligible compared to the duration of a time slot. In other words, we assume that the routing of a packet through the switches and their input links and output links in Figure 1 happens at the beginning (resp., end) of a time slot. For clarity, in the figures in this paper, we use a square filled with dotted (resp., solid) slashes to represent a packet at the beginning (resp., end) of a time slot.

As it requires \( \ell \) time slots for a packet to traverse through a fiber delay line of length \( \ell \), we can view a fiber delay line of length \( \ell \) as a sequential storage element with \( \ell \) contiguous buffers such that each buffer is capable of buffering one packet for one time slot and a packet stored in any one of the \( \ell \) contiguous buffers moves forward to the next contiguous buffer after one time slot until it traverses through the fiber delay line. In Figure 3, we show the \( \ell_i \) contiguous buffers of the fiber delay line in cell \( i \) which are indexed from 0 to \( \ell_i - 1 \) (from left to right), where \( 0 \leq i \leq 2k \). We call buffer \( j \) of cell \( i \) buffer \( b_i(j) \) for \( i = 0, 1, \ldots, 2k \) and \( j = 0, 1, \ldots, \ell_i - 1 \).
Therefore, if a packet, say packet $p$, is routed to the upper output link of switch $i$ at time $t$ (at the beginning of the $t$th time slot) for some $0 \leq i \leq 2k$, then it is stored in buffer $b_i(\ell_i - 1 - j)$ at time $t + j$ (at the end of the $(t + j)$th time slot) for $j = 0, 1, \ldots, \ell_i - 1$ (see Figure 4(a) and Figure 4(b)), and it is available at the upper input link of switch $i$ at time $t + \ell_i$ (at the beginning of the $(t + \ell_i)$th time slot) so that it is routed to the lower output link of switch $i$ at time $t + \ell_i$ (at the beginning of the $(t + \ell_i)$th time slot) when switch $i$ is set to the “cross” state at time $t + \ell_i$ (see Figure 4(c)), and it is routed to the upper output link of switch $i$ at time $t + \ell_i$ (at the beginning of the $(t + \ell_i)$th time slot) and stored in buffer $b_i(\ell_i - 1)$ at time $t + \ell_i$ (at the end of the $(t + \ell_i)$th time slot) when switch $i$ is set to the “bar” state at time $t + \ell_i$ (see Figure 4(d)).

Note that as there are no feedback paths from the output links of a switch to the input links of the other switches with smaller indices, we see that if a packet, say packet $p$, is routed to the upper (resp., lower) input link of switch $i_1$ at time $t$ for some $0 \leq i_1 \leq 2k$, then it can only be routed to the upper output link of switch $i_2$ and stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t$ for some $i_1 \leq i_2 \leq 2k$ (in the case that $i_1 = i_2$, switch $i_1$ must be set to the “bar” (resp., “cross”) state at time $t$; and in the case that $i_1 < i_2$, switch $i_1$ must be set to the “cross” (resp., “bar”) state at time $t$, switch $i$ must be set to the “bar” state at time $t$ for $i = i_1 + 1, i_1 + 2, \ldots, i_2 - 1$, and switch $i_2$ must be set to the “cross” state at time $t$; see Figure 5(a)), or routed to the departure link of the network element in Figure 1 at time $t$ (in this case, switch $i_1$ must be set to the “cross” (resp., “bar”) state at time $t$ and switch $i$ must be set to the “bar” state at time $t$ for $i = i_1 + 1, i_1 + 2, \ldots, 2k$; see Figure 5(b)). Therefore, if a packet is stored in cell $i_1$ at time $t_1$ and is stored in cell $i_2$ at a later time $t_2 > t_1$, then we must have $i_2 \geq i_1$.

To describe the proposed explicit control scheme in this paper, let $q_i(t)$ be the number of packets stored in (the fiber delay line of) cell $i$ in Figure 1 at time $t$ (at the end of the $t$th time slot) for $i = 0, 1, \ldots, 2k$, let $q^{(1)}(t)$ be the total number of packets stored in the first $k$ cells in Figure 1 at time $t$, let $q^{(2)}(t)$ be the total number of packets stored in the last $k + 1$ cells in Figure 1 at time $t$, and let $q(t)$ be the total number of packets stored in the $2k + 1$ cells in Figure 1 at time $t$. Therefore, we have

\[
q^{(1)}(t) = \sum_{i=0}^{k-1} q_i(t), \quad q^{(2)}(t) = \sum_{i=k}^{2k} q_i(t), \quad \text{and} \quad q(t) = q^{(1)}(t) + q^{(2)}(t) = \sum_{i=0}^{2k} q_i(t).
\] (8)
Let $0 \leq i \leq 2k$. If $q_i(t-1) = 0$, then we let $r_i(t) = 0$, $s_i(t) = 0$, and $w_i(t) = 0$. On the other hand, if $q_i(t-1) \neq 0$, then we let $r_i(t)$ and $s_i(t)$ be the indices of the buffers that contain the earliest arrival packet and the latest arrival packet, respectively, among all of the packets stored in cell $i$ at time $t-1$ (at the end of the $(t-1)^{th}$ time slot), and let

$$w_i(t) = (s_i(t) + 1) \mod \ell_i = \begin{cases} s_i(t) + 1, & \text{if } 0 \leq s_i(t) \leq \ell_i - 2, \\ 0, & \text{if } s_i(t) = \ell_i - 1. \end{cases} \quad (9)$$

When $q_i(t-1) \neq 0$ and packet $p'$ is the “latest” arrival packet in cell $i$ at time $t-1$, it is clear from (9) and $0 \leq s_i(t) \leq \ell_i - 1$ that

$$s_i(t) = (w_i(t) - 1) \mod \ell_i = \begin{cases} \ell_i - 1, & \text{if } w_i(t) = 0, \\ w_i(t) - 1, & \text{if } 1 \leq w_i(t) \leq \ell_i - 1, \end{cases} \quad (10)$$

and we immediately see that packet $p'$ is stored in buffer $b_i(\ell_i - 1)$ at time $t-1$ if $w_i(t) = 0$ (see Figure 6(a)), and is stored in buffer $b_i(w_i(t) - 1)$ at time $t-1$ if $w_i(t) \neq 0$ (see Figure 6(b)). For reasons to be explained later, we call $w_i(t)$ the virtual waiting time of cell $i$ at time $t$ in this paper.
Fig. 5. A packet, say packet $p$, that is routed to the input links of switch $i_1$ at time $t$, where $0 \leq i_1 \leq 2k$: (a) Packet $p$ is routed to the upper output link of switch $i_2$ and stored in buffer $b_{i_2}(t_{i_2} - 1)$ at time $t$ for some $i_1 \leq i_2 \leq 2k$; (b) Packet $p$ is routed to the departure link of the network element in Figure 1 at time $t$. 
Fig. 6. The position of the latest arrival packet, say packet $p'$, in cell $i$ at time $t - 1$ when $w_i(t - 1) \neq 0$: (a) $w_i(t) = 0$; (b) $w_i(t) \neq 0$.

The key idea in our explicit control scheme to be described shortly is to operate the network element in Figure 1 such that packets stored in the $2k + 1$ cells satisfy the following ordered and circularly contiguous properties.

(A2) (Ordered property) Packets stored in different cells at any time are ordered according to their arrival times so that if two packets are stored in two different cells at some time, then the earlier arrival packet is stored in the cell with larger index and the later arrival packet is stored in the cell with smaller index. Specifically, if packet $p_1$ arrives at the network element earlier than packet $p_2$, i.e., $p_1 < p_2$, and packet $p_1$ is stored in cell $i_1$ at time $t$ and packet $p_2$ is stored in cell $i_2$ at time $t$ for some $i_1 \neq i_2$, then we have $i_1 > i_2$.

(A3) (Circularly contiguous property) Packets stored in the same cell at any time are labeled sequentially and they are stored in circularly contiguous buffers of that cell according to their arrival times. Specifically, if cell $i$ is nonempty at time $t - 1$ for some $0 \leq i \leq 2k$ and packet $p$ is the “earliest” arrival packet in cell $i$ at time $t - 1$, then packet $p$, packet $p + 1$, …, packet $p + q_i(t - 1) - 1$ are the $q_i(t - 1)$ packets stored in cell $i$ at time $t - 1$, and packet $p + j$ is stored in buffer $b_i((r_i(t) + j) \mod \ell_i)$ at time $t - 1$ for $j = 0, 1, \ldots, q_i(t - 1) - 1$ as shown in Figure 7.

Fig. 7. The circularly contiguous property in (A3) at time $t - 1$ when $q_i(t - 1) \neq 0$: (a) $r_i(t) + q_i(t - 1) \leq \ell_i$; (b) $r_i(t) + q_i(t - 1) > \ell_i$. 
The following lemma can be easily obtained by using the circularly contiguous property in (A3).

**Lemma 2** Suppose that the circularly contiguous property in (A3) is satisfied at time \( t - 1 \) and \( 0 \leq i \leq 2k \).

(i) Assume that \( r_i(t) + q_i(t - 1) \leq \ell_i \) and \( r_i(t) \neq 0 \). Then buffer \( b_i(0) \) is empty at time \( t - 1 \).

(ii) Assume that \( r_i(t) + q_i(t - 1) > \ell_i \). Then buffer \( b_i(0) \) is nonempty at time \( t - 1 \).

**Proof.** (i) As \( r_i(t) \neq 0 \), we have from the definition of \( r_i(t) \) that \( q_i(t - 1) \neq 0 \). Let packet \( p \) be the “earliest” arrival packet in cell \( i \) at time \( t - 1 \). Since the circularly contiguous property in (A3) is satisfied at time \( t - 1 \), we then see from \( r_i(t) + q_i(t - 1) \leq \ell_i \) that packet \( p + j \) is stored in buffer \( b_i(r_i(t) + j) \) at time \( t - 1 \) for \( j = 0, 1, \ldots, q_i(t - 1) - 1 \). As such, it follows from \( r_i(t) \geq 1 \) and \( r_i(t) + q_i(t - 1) - 1 \leq \ell_i - 1 \) that buffer \( b_i(0) \) is empty at time \( t - 1 \) (see Figure 7(a)).

(ii) As there can be at most \( \ell_i \) packets stored in cell \( i \) at any time, we have \( q_i(t - 1) \leq \ell_i \). From \( 0 \leq r_i(t) \leq \ell_i - 1, 0 \leq q_i(t - 1) \leq \ell_i \), and \( r_i(t) + q_i(t - 1) > \ell_i \), we can see that \( r_i(t) \geq 1 \) and \( q_i(t - 1) \geq 2 \). Let packet \( p \) be the “earliest” arrival packet in cell \( i \) at time \( t - 1 \). Since the circularly contiguous property in (A3) is satisfied at time \( t - 1 \), we then see from \( r_i(t) + q_i(t - 1) > \ell_i \) that packet \( p + j \) is stored in buffer \( b_i(r_i(t) + j) \) at time \( t - 1 \) for \( j = 0, 1, \ldots, \ell_i - 1 - r_i(t) \) and is stored in buffer \( b_i(r_i(t) + j - \ell_i) \) at time \( t - 1 \) for \( j = \ell_i - r_i(t), \ell_i - r_i(t) + 1, \ldots, q_i(t - 1) - 1 \). In particular, packet \( p + \ell_i - r_i(t) \) is stored in buffer \( b_i(0) \) at time \( t - 1 \), and hence buffer \( b_i(0) \) is nonempty at time \( t - 1 \) (see Figure 7(b)).

Now we explain why we call \( w_i(t) \) as given in (9) the virtual waiting time of cell \( i \) at time \( t \). If \( q_i(t - 1) = 0 \), then we define the virtual waiting time \( w'_i(t) \) of cell \( i \) at time \( t \) as zero. As in this case we also define \( w_i(t) \) as zero, we have \( w'_i(t) = w_i(t) = 0 \) in this case.

On the other hand, if \( q_i(t - 1) \neq 0 \), then let packet \( p' \) be the “latest” arrival packet in cell \( i \) at time \( t \). Consider the scenario that packet \( p' + 1 \) is in the network element in Figure 1 at time \( t \). Then we define the virtual waiting time \( w'_i(t) \) of cell \( i \) at time \( t \) as the time that packet \( p' + 1 \) must wait (with respect to time \( t \)) until packet \( p' \) and packet \( p' + 1 \) can be routed consecutively to the same output link of switch \( i \) at time \( t + w'_i(t) - 1 \) and time \( t + w'_i(t) \), respectively. The intuition behind the definition of the virtual waiting time in this case is that by so doing, it is then possible to operate the network element in Figure 1 such that the circularly contiguous property in (A3) is satisfied at all times as will be shown later in the proof of Theorem 15. For the case that \( w_i(t) = 0 \), we see from (10) that packet \( p' \) is stored in buffer \( b_i(\ell_i - 1) \) at time \( t - 1 \), implying that packet \( p' \) is routed to the upper output link of switch \( i \) at time \( t - 1 \). Thus, we can route packet \( p' + 1 \) to the upper output link of switch \( i \) at time \( t \) (this can be achieved under our explicit control scheme in (C1)–(C3) described below and is shown later in Lemma 6(i)) so that packet \( p' \) and packet \( p' + 1 \) are routed consecutively to the upper output link of switch \( i \) at time \( t - 1 \) and time \( t \), respectively (see Figure 8(a)). Therefore, the virtual waiting time \( w'_i(t) \)
of cell $i$ at time $t$ is equal to zero, and we have $w_i'(t) = w_i(t) = 0$ in this case. For the case that $w_i(t) \neq 0$, we see from (10) that packet $p'$ is stored in buffer $b_i(w_i(t) - 1)$ at time $t - 1$. As it is clear from (9) that $w_i(t) \leq \ell_i - 1$, we see that $w_i(t) - 1 \neq \ell_i - 1$ and hence packet $p'$ is not stored in buffer $b_i(\ell_i - 1)$ at time $t - 1$, implying that packet $p'$ is not routed to the upper output link of switch $i$ at time $t - 1$. Since it is clear that packet $p'$ is at the upper input link of switch $i$ at time $t + w_i(t) - 1$, it then follows that packet $p'$ is routed to one of the two output links of switch $i$ at time $t + w_i(t) - 1$. Thus, we can route packet $p' + 1$ to the same output link of switch $i$ at time $t + w_i(t)$, depending on which output link of switch $i$ packet $p'$ is routed to at time $t + w_i(t) - 1$ (this can also be achieved under our explicit control scheme in (C1)–(C3) described below and is shown later in Lemma 6(i)), so that packet $p'$ and packet $p' + 1$ are routed consecutively to the same output link of switch $i$ at time $t + w_i(t) - 1$ and time $t + w_i(t)$, respectively (see Figure 8(b) and Figure 8(c)). Therefore, the virtual waiting time $w_i'(t)$ of cell $i$ at time $t$ is also equal to $w_i(t)$ in this case.

We need to introduce the $C$-transform in [14] that will be used in our proposed control scheme.

**Definition 3 (C-transform [14])** Let $\ell_i$ be a positive integer for $i = 0, 1, \ldots, k - 1$. The $C$-transform of a nonnegative integer $x$ with respect to the $k$-vector $\ell_0^{-1} = (\ell_0, \ell_1, \ldots, \ell_{k-1})$ is defined as the $k$-vector $C(x; \ell_0^{-1}) = (I_0(x; \ell_0^{k-1}), I_1(x; \ell_0^{k-1}), \ldots, I_{k-1}(x; \ell_0^{k-1}))$, where $I_{k-1}(x; \ell_0^{k-1})$, $I_{k-2}(x; \ell_0^{k-1}), \ldots, I_0(x; \ell_0^{k-1})$ (in that order) are given recursively by

$$I_i(x; \ell_0^{k-1}) = \begin{cases} 1, & \text{if } x - \sum_{j=i+1}^{k-1} I_j(x; \ell_0^{k-1}) \ell_j \geq \ell_i, \\ 0, & \text{otherwise}, \end{cases}$$  

with the convention that the sum in (11) is 0 if the upper index is smaller than its lower index.

It is clear that the $C$-transform is a generalization of the well-known binary representation, and it was shown in [14] that the $C$-transform has the unique representation property such that $x = \sum_{i=0}^{k-1} I_i(x; \ell_0^{k-1}) \ell_i$ for $x = 0, 1, \ldots, \sum_{i=0}^{k-1} \ell_i$ if and only if $\ell_0^{k-1} \in A_k$.

We now describe the proposed control scheme. Initially, we have $q_i(0) = 0$ for $i = 0, 1, \ldots, 2k$ as the network element is started from an empty system at time 0. At every time $t \geq 1$, we set the connection patterns of the $1 \times 2$ optical crossbar switch and the $2k + 1$ $2 \times 2$ optical crossbar switches according to the following explicit control scheme, where we denote $c_i(t) \in \{\text{cross, bar}\}$ as the connection pattern of switch $i$ at time $t$ for $i = 0, 1, \ldots, 2k$.

**(C1) The connection pattern of the $1 \times 2$ switch:** As mentioned in Section II, the $1 \times 2$ optical crossbar switch in Figure 1 is used for admission control so that the maximum buffer usage property in (P3) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times. We connect the input link of the $1 \times 2$ optical crossbar switch to its upper output link at time $t$ when $q(t - 1) - c(t) < \sum_{j=k}^{2k} \ell_j$ (as we will show in the proof of Theorem 15 that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times, it is clear that in this case an arrival packet from the arrival link at time $t$ can be
admitted into the network element without overflowing the buffer of the network element), and connect the input link of the $1 \times 2$ optical crossbar switch to its lower output link at time $t$ when $q(t - 1) - c(t) \geq \sum_{j=k}^{2k} \ell_j$ (as we will show in Remark 16 that $q(t) \leq \sum_{j=k}^{2k} \ell_j$ for all $t \geq 0$, it is clear that in this case the condition $q(t - 1) - c(t) \geq \sum_{j=k}^{2k} \ell_j$ can be replaced by $q(t - 1) - c(t) = \sum_{j=k}^{2k} \ell_j$, and hence an arrival packet from the arrival link at time $t$ is dropped through the loss link since the buffer of the network element will be overflowed once the arrival packet is admitted into the network element). Therefore, we have

$$a_0(t) = \begin{cases} a(t), & \text{if } q(t - 1) - c(t) < \sum_{j=k}^{2k} \ell_j, \\ 0, & \text{if } q(t - 1) - c(t) \geq \sum_{j=k}^{2k} \ell_j, \end{cases} \quad (12)$$
\[ \ell(t) = \begin{cases} 0, & \text{if } q(t-1) - c(t) < \sum_{j=k}^{2k} \ell_j, \\ a(t), & \text{if } q(t-1) - c(t) \geq \sum_{j=k}^{2k} \ell_j. \end{cases} \]  

(C2) The connection patterns of the first \( k \) \( 2 \times 2 \) switches: If \( q^{(1)}(t-1) = 0 \), then let \( j(t) \) be the smallest index of a nonempty cell among the last \( k+1 \) cells at time \( t-1 \) when the last \( k+1 \) cells are nonempty at time \( t-1 \), and let \( j(t) = 2k \) when the last \( k+1 \) cells are empty at time \( t-1 \), i.e.,

\[ j(t) = \begin{cases} \min\{k \leq i \leq 2k : q_i(t-1) \neq 0\}, & \text{if } q^{(2)}(t-1) \neq 0, \\ 2k, & \text{if } q^{(2)}(t-1) = 0. \end{cases} \]

We set the connection patterns of the first \( k \) \( 2 \times 2 \) switches at time \( t \) according to the \( C \)-transform \( (I_0(w_{j(t)}(t); \ell_0^{k-1}), I_1(w_{j(t)}(t); \ell_1^{k-1}), \ldots, I_{k-1}(w_{j(t)}(t); \ell_{k-1}^{k-1})) \) of the virtual waiting time \( w_{j(t)}(t) \) of cell \( j(t) \) at time \( t \) with respect to the \( k \)-vector \( \ell_0^{k-1} = (\ell_0, \ell_1, \ldots, \ell_{k-1}) \) (note that as it is clear from (14) that \( k \leq j(t) \leq 2k \), we see from (9), (4), and (2) that that \( w_{j(t)}(t) \leq \ell_j(t) - 1 \leq \ell_k - 1 \leq \sum_{i=0}^{k-1} \ell_i \) and hence \( k \) digits are enough for the \( C \)-transform of \( w_{j(t)}(t) \)). Specifically, the connection pattern of switch \( i \) is set to the “cross” state at time \( t \) if \( I_i(w_{j(t)}(t); \ell_0^{k-1}) = 1 \), and is set to the “bar” state at time \( t \) if \( I_i(w_{j(t)}(t); \ell_0^{k-1}) = 0 \) for \( i = 0, 1, \ldots, k-1 \). Therefore, we have

\[ c_i(t) = \begin{cases} \text{cross}, & \text{if } I_i(w_{j(t)}(t); \ell_0^{k-1}) = 1, \\ \text{bar}, & \text{if } I_i(w_{j(t)}(t); \ell_0^{k-1}) = 0, \end{cases} \]

for \( i = 0, 1, \ldots, k-1 \).

On the other hand, if \( q^{(1)}(t-1) \neq 0 \), then let \( n(t) \) be the number of nonempty cells among the first \( k \) cells at time \( t-1 \) and let \( 0 \leq j_1(t) < j_2(t) < \cdots < j_{n(t)}(t) \leq k-1 \) be the indices of these nonempty cells. We set the connection patterns of the \( 2 \times 2 \) switches in these nonempty cells to the “cross” state at time \( t \). The connection patterns of the other \( 2 \times 2 \) switches among the first \( k \) \( 2 \times 2 \) switches at time \( t \) are specified as follows. For convenience, let \( j_0(t) = -1 \). For \( j_{h-1}(t) + 1 \leq i \leq j_h(t) - 1 \) and \( 1 \leq h \leq n(t) \), the connection pattern of switch \( i \) at time \( t \) is set according to the \( C \)-transform \( (I_0(w_{j_h(t)}(t); \ell_0^{j_h(t)-1}), I_1(w_{j_h(t)}(t); \ell_0^{j_h(t)-1}), \ldots, I_{j_h(t)-1}(w_{j_h(t)}(t); \ell_0^{j_h(t)-1})) \) of the virtual waiting time \( w_{j_h(t)}(t) \) of cell \( j_h(t) \) at time \( t \) with respect to the \( j_h(t) \)-vector \( \ell_0^{j_h(t)-1} = (\ell_0, \ell_1, \ldots, \ell_{j_h(t)-1}) \). Specifically, the connection pattern of switch \( i \) is set to the “cross” state at time \( t \) if \( I_i(w_{j_h(t)}(t); \ell_0^{j_h(t)-1}) = 1 \), and is set to the “bar” state at time \( t \) if \( I_i(w_{j_h(t)}(t); \ell_0^{j_h(t)-1}) = 0 \) for \( j_{h-1}(t) + 1 \leq i \leq j_h(t) - 1 \) and \( 1 \leq h \leq n(t) \). Furthermore, for \( j_{n(t)}(t) + 1 \leq i \leq k-1 \), the connection pattern of switch \( i \) at time \( t \) remains the same as that at time \( t-1 \) if there is no packet at the output link of switch \( k-1 \) at time \( t-1 \), i.e., \( d_{k-1}(t-1) = 0 \), and is set to the “bar” state at time \( t \) if there is a packet at the output link of switch \( k-1 \) at time \( t-1 \), i.e., \( d_{k-1}(t-1) = 1 \). Therefore, we have

\[ c_i(t) = \text{cross}, \]
for \( i = j_1(t), j_2(t), \ldots, j_n(t) \),
\[
c_i(t) = \begin{cases} 
\text{cross}, & \text{if } I_i(w_{j_i(t)}(t); \ell_0^{j_i(t)-1}) = 1, \\
\text{bar}, & \text{if } I_i(w_{j_i(t)}(t); \ell_0^{j_i(t)-1}) = 0,
\end{cases}
\]
for \( j_{h-1}(t) + 1 \leq i \leq j_h(t) - 1 \) and \( 1 \leq h \leq n(t) \), and
\[
c_i(t) = \begin{cases} 
c_i(t-1), & \text{if } d_{k-1}(t-1) = 0, \\
\text{bar}, & \text{if } d_{k-1}(t-1) = 1,
\end{cases}
\]
for \( j_{n(t)}(t) + 1 \leq i \leq k - 1 \).

(C3) The connection patterns of the last \( k + 1 \) 2 x 2 switches: Let \( k \leq i \leq 2k \). As we will show in Lemma 14 that when \( c(t) = 1 \) and \( \sum_{j=i+1}^{2k} q_j(t-1) > 0 \), the departure packet from the network element at time \( t \) is the earliest arrival packet in the last \( 2k - i \) cells, i.e., cell \( i + 1 \), cell \( i + 2 \), \ldots, cell \( 2k \), at time \( t - 1 \), it then follows that \( \sum_{j=i+1}^{2k} q_j(t-1) - c(t) \) is the occupied buffer space in front of cell \( i \) at time \( t \) in this case. If \( q_i(t-1) = 0 \), then we set the connection pattern of switch \( i \) to the “bar” state at time \( t \) when there is available buffer space in front of cell \( i \) at time \( t \), i.e., \( \sum_{j=i+1}^{2k} q_j(t-1) - c(t) < \sum_{j=i+1}^{2k} \ell_j \), and set the connection pattern of switch \( i \) to the “cross” state at time \( t \) when there is no available buffer space in front of cell \( i \) at time \( t \), i.e., \( \sum_{j=i+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i+1}^{2k} \ell_j \). Therefore, we have
\[
c_i(t) = \begin{cases} 
\text{bar}, & \text{if } \sum_{j=i+1}^{2k} q_j(t-1) - c(t) < \sum_{j=i+1}^{2k} \ell_j, \\
\text{cross}, & \text{if } \sum_{j=i+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i+1}^{2k} \ell_j.
\end{cases}
\]

On the other hand, if \( q_i(t-1) \neq 0 \), then we set the connection pattern of switch \( i \) to the “cross” state at time \( t \) when the earliest arrival packet in cell \( i \) at time \( t - 1 \) is stored in buffer \( b_i(0) \) at time \( t - 1 \) and there is available buffer space in front of cell \( i \) at time \( t \), i.e., \( r_i(t) = 0 \) and \( \sum_{j=i+1}^{2k} q_j(t-1) - c(t) < \sum_{j=i+1}^{2k} \ell_j \), set the connection pattern of switch \( i \) to the “bar” state at time \( t \) when the earliest arrival packet in cell \( i \) at time \( t - 1 \) is stored in buffer \( b_i(0) \) at time \( t - 1 \) and there is no available buffer space in front of cell \( i \) at time \( t \), i.e., \( r_i(t) = 0 \) and \( \sum_{j=i+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i+1}^{2k} \ell_j \), set the connection pattern of switch \( i \) to the “cross” state at time \( t \) when the earliest arrival packet in cell \( i \) at time \( t - 1 \) is not stored in buffer \( b_i(0) \) at time \( t - 1 \), i.e., \( r_i(t) \neq 0 \), and \( r_i(t) + q_i(t-1) \leq \ell_i \), and set the connection pattern of switch \( i \) to the “bar” state at time \( t \) when the earliest arrival packet in cell \( i \) at time \( t - 1 \) is not stored in buffer \( b_i(0) \) at time \( t - 1 \), i.e., \( r_i(t) \neq 0 \), and \( r_i(t) + q_i(t-1) > \ell_i \). Therefore, we have
\[
c_i(t) = \begin{cases} 
\text{cross}, & \text{if } r_i(t) = 0 \text{ and } \sum_{j=i+1}^{2k} q_j(t-1) - c(t) < \sum_{j=i+1}^{2k} \ell_j, \\
\text{bar}, & \text{if } r_i(t) = 0 \text{ and } \sum_{j=i+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i+1}^{2k} \ell_j, \\
\text{cross}, & \text{if } r_i(t) \neq 0 \text{ and } r_i(t) + q_i(t-1) \leq \ell_i, \\
\text{bar}, & \text{if } r_i(t) \neq 0 \text{ and } r_i(t) + q_i(t-1) > \ell_i.
\end{cases}
\]

Suppose that \( \ell_0^{k-1} \in A_k \), (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3).
Clearly, from the description in (C1), we see that the maximum buffer usage property in (P3) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times. In Lemma 4 below, we will show that there is no conflict inside the network element and hence the flow conservation property in (P1) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times. Furthermore, from the ordered property in (A2) and the circularly contiguous property in (A3), we can show that the nonidling property in (P2) of Definition 1 and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ are also satisfied at all times.

**Lemma 4** Suppose that the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Then there is no conflict at any input link or output link of the switches and at any buffer of the cells in Figure 1 at any time, i.e., there is at most one packet at any input link or output link of the switches and there is at most one packet stored in any buffer of the cells in Figure 1 at any time. Therefore, the $1 \times 2$ optical crossbar switch and the $2k + 1$ cells in Figure 1 satisfy the following flow conservation property at all times: Packets from the input link of the $1 \times 2$ optical crossbar switch are transmitted through its two output links, and packets from the input link of cell $i$ are either stored in the fiber delay line in cell $i$ or transmitted through the output link of cell $i$ for $i = 0, 1, \ldots, 2k$, and hence we have

$$a(t) = a_0(t) + \ell(t), \text{ for } t \geq 0,$$

$$q_i(t) = q_i(t - 1) + a_i(t) - d_i(t), \text{ for } t \geq 1 \text{ and } 0 \leq i \leq 2k.$$

Furthermore, packets from the arrival link of the network element are either stored in the $2k + 1$ cells or transmitted through the departure link or the loss link of the network element, namely, the flow conservation property in (P1) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times.

**Proof.** First consider the $1 \times 2$ optical crossbar switch in Figure 1. As there is at most one arrival packet at its input link and we have from the explicit control scheme in (C1) that packets at its output links can only come from its input link, it is immediate that there is no conflict at any input link or output link of the $1 \times 2$ optical crossbar switch at any time, and hence we have $a(t) = a_0(t) + \ell(t)$ for $t \geq 0$ in (21).

Now consider switch $i$ in Figure 1, where $0 \leq i \leq 2k$. Suppose that there is no conflict at the lower input link of switch $i$ at time $t$ for all $t \geq 0$. We show by induction on time $t$ that there is no conflict at the upper input link and the two output links of switch $i$ and at any buffer of cell $i$ at time $t$ for all $t \geq 0$. Since the network element in Figure 1 is started from an empty system at time 0, there is no conflict at the upper input link and the two output links of switch $i$ and at any buffer of cell $i$ at time 0. Assume as the induction hypothesis that there is no conflict at the upper input link and the two output links of switch $i$ and at any buffer of cell $i$ at some time $t - 1 \geq 0$. As packet at the upper input link of switch $i$ at time $t$ is the packet stored in buffer
$b_i(0)$ at time $t - 1$, we see from the induction hypothesis that there is no conflict at the upper input link of switch $i$ at time $t$. As we also suppose that there is no conflict at the lower input link of switch $i$ at time $t$, it is clear that there is no conflict at the two output links of switch $i$ at time $t$ no matter switch $i$ is set to the “cross” state or the “bar” state at time $t$. Furthermore, since the packet stored in buffer $b_i(j)$ at time $t$ is the packet stored in buffer $b_i(j + 1)$ at time $t - 1$ for $j = 0, 1, \ldots, \ell_i - 2$, it follows from the induction hypothesis that there is no conflict at buffer $b_i(j)$ at time $t$ for $j = 0, 1, \ldots, \ell_i - 2$. Moreover, since the packet stored in buffer $b_i(\ell_i - 1)$ at time $t$ is the packet at the upper output link of switch $i$ at time $t$ and we have already shown that there is no conflict at the upper output link of switch $i$ at time $t$, it follows that there is no conflict at buffer $b_i(\ell_i - 1)$ at time $t$, and the induction is completed.

As the lower input link of switch 0 is connected to the upper output link of the $1 \times 2$ optical crossbar switch and we have already shown that there is no conflict at the upper output link of the $1 \times 2$ optical crossbar switch at any time, it is clear that there is no conflict at the lower input link of switch 0 at any time, and we immediately see from the argument in the above paragraph that there is no conflict at the upper input link and the two output links of switch 0 and at any buffer of cell 0 at any time. Similarly, since the lower input link of switch 1 is connected to the lower output link of switch 0 and hence there is no conflict at the lower input link of switch 1 at any time, we can see from the argument in the above paragraph that there is no conflict at the upper input link and the two output links of switch 1 and at any buffer of cell 1 at any time. Repeating the above argument for $2k + 1$ times, we see that there is no conflict at any input link or output link of switch $i$ and at any buffer of cell $i$ at any time for $0 \leq i \leq 2k$, and hence we have $q_i(t) = q_i(t - 1) + a_i(t) - d_i(t)$ for $t \geq 1$ and $0 \leq i \leq 2k$ in (22).

\textbf{Lemma 5} Suppose that the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)--(C3).

(i) A packet is routed into each fiber delay line in the first $k$ cells at most once.

(ii) Packets stored in the first $k$ cells satisfy the ordered property in (A2) at all times. Furthermore, packets stored in any one of the first $k$ cells at any time are ordered according to their arrival times and they depart from the output link of that cell in the FIFO order. Specifically, if packet $p_1$ arrives at the network element earlier than packet $p_2$, i.e., $p_1 < p_2$, and packet $p_1$ is stored in buffer $b_i(j_1)$ at time $t$ and packet $p_2$ is stored in buffer $b_i(j_2)$ at time $t$ for some $0 \leq i \leq k - 1$, then we have $j_1 < j_2$ and packet $p_1$ departs from the output link of cell $i$ earlier than packet $p_2$. Equivalently, packets stored in any one of the first $k$ cells depart from the output link of that cell in the FIFO order at any time, i.e., if there is a packet routed from the fiber delay line in cell $i$ to its output link at time $t$ for some $0 \leq i \leq k - 1$, then it is the “earliest” arrival packet in cell $i$ at time $t - 1$.

(iii) If there is a packet at the output link of cell $k - 1$ at time $t$, then it must be the earliest arrival packet among all of the packets that are either stored in the first $k$ cells at time $t - 1$ or admitted into the network element at time $t$.  

there are only three possibilities to consider.

Proof. (i) Suppose that \(0 \leq i \leq k - 1\) and a packet, say packet \(p\), is routed into the fiber delay line in cell \(i\) for the first time at time \(t\). Then it is clear that packet \(p\) is stored in buffer \(b_i(\ell_i - 1 - j)\) at time \(t + j\) for \(j = 0, 1, \ldots, \ell_i - 1\). As \(0 \leq i \leq k - 1\) and cell \(i\) is nonempty at time \(t + \ell_i - 1\), we see from (16) that switch \(i\) is set to the “cross” state at time \(t + \ell_i\). It then follows that packet \(p\) will be either routed into the fiber delay line in cell \(i\) or stored in buffer \(b_i(\ell_i - 1 - j)\) at time \(t + j\) for \(j = 0, 1, \ldots, \ell_i - 1\). As such, packet \(p\) will be stored in cells with indices greater than \(i\) after time \(t + \ell_i - 1\) before it departs from the departure link of the network element. Therefore, packet \(p\) cannot be routed into the fiber delay line in cell \(i\) again after time \(t\).

(ii) We prove Lemma 5(ii) by induction on time \(t \geq 0\). Since the network element in Figure 1 is started from an empty system at time 0, Lemma 5(ii) holds vacuously at time 0. Assume as the induction hypothesis that Lemma 5(ii) holds at some time \(t - 1 \geq 0\). If there is at most one packet stored in the first \(k\) cells at time \(t\), then there is nothing to prove. On the other hand, if there are at least two packets stored in the first \(k\) cells at time \(t\), then we consider two such packets, say packet \(p_1\) and packet \(p_2\), and packet \(p_1\) arrives at the network element earlier than packet \(p_2\), i.e., \(p_1 < p_2\). Since there is at most one arrival packet from the arrival link of the network element at any time, packet \(p_1\) must have arrived at the network element before time \(t\), and we assume that packet \(p_1\) is stored in buffer \(b_{i_1}(j_1)\) at time \(t - 1\) for some \(0 \leq i_1 \leq k - 1\) and \(0 \leq j_1 \leq \ell_{i_1} - 1\). Also, it is clear that packet \(p_2\) either has not arrived at the network element at time \(t - 1\) (in this case packet \(p_2\) must arrive at the network element at time \(t\) and be admitted into the network element at time \(t\) as it is stored in the first \(k\) cells at time \(t\) or is stored in buffer \(b_{i_2}(j_2)\) at time \(t - 1\), where we have from the induction hypothesis that either \((i_2 < i_1\) and \(0 \leq j_2 \leq \ell_{i_2} - 1)\) or \((i_2 = i_1\) and \(j_1 < j_2 \leq \ell_{i_2} - 1)\). Note from (16) that switch \(i_1\) and switch \(i_2\) (in the case that packet \(p_2\) is stored in buffer \(b_{i_2}(j_2)\) at time \(t - 1\) are set to the “cross” state at time \(t\). We then consider the two cases \(j_1 = 0\) and \(j_1 \neq 0\) separately.

**Case 1:** \(j_1 = 0\). Since switch \(i_1\) is set to the “cross” state at time \(t\) and we know that packet \(p_1\) and packet \(p_2\) are stored in the first \(k\) cells at time \(t\), we see that in this case packet \(p_1\) must be routed to the fiber delay line in cell \(i'_1\) and stored in buffer \(b_{i_1}(\ell_{i_1} - 1)\) at time \(t\) for some \(i_1 < i'_1 \leq k - 1\) and packet \(p_2\) can only be stored in cell \(i'_2\) at time \(t\) for some \(0 \leq i'_2 \leq i_1\). It follows from \(i'_2 < i'_1\) that packet \(p_1\) and packet \(p_2\) satisfy the ordered property in (A2) at time \(t\). Therefore, Lemma 5(ii) holds at time \(t\) in this case.

**Case 2:** \(j_1 \neq 0\). Since switch \(i_1\) is set to the “cross” state at time \(t\), we see that in this case packet \(p_1\) is stored in buffer \(b_{i_1}(j_1 - 1)\) at time \(t\) and packet \(p_2\) can only be stored in cell \(i'_2\) at time \(t\) for some \(0 \leq i'_2 \leq i_1\). If \(i'_2 < i_1\), then packet \(p_1\) and packet \(p_2\) satisfy the ordered property in (A2) at time \(t\). Therefore, Lemma 5(ii) holds at time \(t\) in this case. Otherwise, if \(i'_2 = i_1\), then there are only three possibilities to consider.

**Subcase 2(a):** Packet \(p_2\) is admitted into the network element at time \(t\) and switch \(i\) is set to the “bar” state at time \(t\) for \(i = 0, 1, \ldots, i_1 - 1\). Since switch \(i_1\) is set to the “cross” state at
time $t$, in this subcase it is clear that packet $p_2$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1 - j)$ at time $t + j$ for $j = 0, 1, \ldots, \ell_{i_1} - 1$. From (16), we can see that switch $i_1$ is set to the “cross” state during the time period $[t + 1, t + \ell_{i_1}]$, and hence packet $p_1$ departs from the output link of cell $i_1$ at time $t + j$ and packet $p_2$ departs from the output link of cell $i_2$ at time $t + \ell_{i_1}$. As such, it follows from $j_1 < \ell_{i_1}$ that packet $p_1$ and packet $p_2$ are ordered according to their arrival times when they are stored in cell $i_1$ at time $t$ and they depart from the output link of cell $i_1$ in the FIFO order. Therefore, Lemma 5(ii) holds at time $t$ in this subcase.

Subcase 2(b): Packet $p_2$ is stored in buffer $b_{i_2}(0)$, where $i_2 < i_1$, at time $t - 1$ and switch $i$ is set to the “bar” state at time $t$ for $i = i_2 + 1, i_2 + 2, \ldots, i_1 - 1$. Since switch $i_1$ and switch $i_2$ are set to the “cross” state at time $t$, in this subcase it is clear that packet $p_2$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1 - j)$ at time $t + j$ for $j = 0, 1, \ldots, \ell_{i_1} - 1$. By the same argument as in Subcase 2(a) above, we can also show that Lemma 5(ii) holds at time $t$ in this subcase.

Subcase 2(c): Packet $p_2$ is stored in buffer $b_{i_1}(j_2)$, where $j_1 < j_2 \leq \ell_{i_1} - 1$, at time $t - 1$. In this subcase, it is clear that packet packet $p_2$ is stored in buffer $b_{i_1}(j_2 - 1 - j)$ at time $t + j$ for $j = 0, 1, \ldots, j_2 - 1$. From (16), we can see that switch $i_1$ is set to the “cross” state during the time period $[t + 1, t + j_2]$, and hence packet $p_1$ departs from the output link of cell $i_1$ at time $t + j$ and packet $p_2$ departs from the output link of cell $i_1$ at time $t + j_2$. As such, it follows from $j_1 < j_2$ that packet $p_1$ and packet $p_2$ are ordered according to their arrival times when they are stored in cell $i_1$ at time $t$ and they depart from the output link of cell $i_1$ in the FIFO order. Therefore, Lemma 5(ii) holds at time $t$ in this subcase.

(iii) Suppose that there is a packet, say packet $p$, at the output link of cell $k - 1$ at time $t$. If the first $k$ cells are empty at time $t - 1$, then it must be the case that packet $p$ is admitted into the network element at time $t$ and the first $k$ switches are set to the “bar” state at time $t$ so that packet $p$ is routed to the output link of cell $k - 1$ at time $t$.

On the other hand, if the first $k$ cells are nonempty at time $t - 1$, then let $n(t)$ be the number of nonempty cells among the first $k$ cells at time $t - 1$ and let $0 \leq j_1(t) < j_2(t) < \cdots < j_{n(t)}(t) \leq k - 1$ be the indices of these nonempty cells. As cell $j_{n(t)}(t)$ is nonempty, cell $i$ is empty for $i = j_{n(t)}(t) + 1, j_{n(t)}(t) + 2, \ldots, k - 1$, and we have from (16) that switch $j_{n(t)}(t)$ is set to the “cross” state at time $t$, it must be the case that packet $p$ is stored in buffer $b_{j_{n(t)}(t)}(0)$ at time $t - 1$ and switch $i$ is set to the “bar” state at time $t$ for $i = j_{n(t)}(t) + 1, j_{n(t)}(t) + 2, \ldots, k - 1$ so that packet $p$ is routed to the output link of cell $k - 1$ at time $t$. Since packet $p$ is stored in buffer $b_{j_{n(t)}(t)}(0)$ at time $t - 1$ and cell $i$ is empty at time $t - 1$ for $i = j_{n(t)}(t) + 1, j_{n(t)}(t) + 2, \ldots, k - 1$, we see from Lemma 5(ii) that packet $p$ is the earliest arrival packet stored in the first $k$ cells at time $t - 1$.

**Lemma 6** Suppose that $\ell_{i_0}^{k-1} \in A_k$, (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the ordered property in (A2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ are satisfied up to time $t - 1$. 
Assume that there is a packet admitted into the network element at time $t_0$ and the $2k + 1$ cells are nonempty at time $t_0 - 1$ for some $t_0 \leq t$, say packet $p'$ is the “latest” arrival packet in the $2k + 1$ cells at time $t_0 - 1$ and hence packet $p' + 1$ is the packet admitted into the network element at time $t_0$ (note that as we assume that the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied up to time $t - 1$ and packet $p'$ is stored in the $2k + 1$ cells at time $t_0 - 1$, it is clear that any packet that arrives later than packet $p'$ must arrive after time $t_0 - 1$ since otherwise such a packet will still be stored in the $2k + 1$ cells at time $t_0 - 1$ and hence packet $p'$ cannot be the latest arrival packet in the $2k + 1$ cells at time $t_0 - 1$). We assume that packet $p'$ is stored in cell $i_1$ at time $t_0 - 1$ for some $0 \leq i_1 \leq 2k$.

(i) Suppose that packet $p'$ is stored in the first $k$ cells at time $t_0 - 1$, i.e., $0 \leq i_1 \leq k - 1$. Then packet $p' + 1$ is routed to the input link of cell $i_1$ at time $t_0 + w_{i_1}(t_0)$. Furthermore, if $w_{i_1}(t_0) = 0$, then packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i_1$ consecutively at time $t_0 + \ell_{i_1} - 1$ and time $t_0 + \ell_{i_1}$, respectively; otherwise, if $w_{i_1}(t_0) \neq 0$, then packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i_1$ consecutively at time $t_0 + w_{i_1}(t_0) - 1$ and time $t_0 + w_{i_1}(t_0)$, respectively.

(ii) Suppose that packet $p'$ is stored in the last $k + 1$ cells at time $t_0 - 1$, i.e., $k \leq i_1 \leq 2k$. Then packet $p' + 1$ is routed to the output link of cell $k - 1$ at time $t_0 + w_{i_1}(t_0)$.

(iii) Suppose that packet $p'$ is stored in the first $k$ cells at time $t_0 - 1$, i.e., $0 \leq i_1 \leq k - 1$. If packet $p'$ is stored in the first $k$ cells at time $t - 1$, say packet $p'$ is stored in cell $i_2$ at time $t - 1$ for some $i_1 \leq i_2 \leq k - 1$ (note that $t_0 \leq t$), then packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i$ consecutively at or before time $t$ for $i = i_1, i_1 + 1, \ldots, i_2 - 1$; otherwise, if packet $p'$ is not stored in the first $k$ cells at time $t - 1$, then packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i$ consecutively at or before time $t$ for $i = i_1, i_1 + 1, \ldots, k - 1$.

**Proof.** (i) Since we assume that the ordered property in (A2) is satisfied at time $t_0 - 1$ (note that $t_0 - 1 \leq t - 1$) and packet $p'$ is the latest arrival packet in the $2k + 1$ cells at time $t_0 - 1$ and is stored in cell $i_1$ at time $t_0 - 1$, it is easy to see that

$$q_i(t_0 - 1) = 0, \text{ for } 0 \leq i \leq i_1 - 1,$$  \hspace{1cm} (23)

and

$$q_{i_1}(t_0 - 1) \neq 0.$$  \hspace{1cm} (24)

It follows from (8), $0 \leq i_1 \leq k - 1$, (23), and (24) that

$$q^{(1)}(t_0 - 1) = \sum_{i=0}^{k-1} q_i(t_0 - 1) \neq 0,$$  \hspace{1cm} (25)

and the smallest index $j_1(t_0)$ of a nonempty cell among the first $k$ cells at time $t_0 - 1$ is given by

$$j_1(t_0) = i_1.$$  \hspace{1cm} (26)
We then consider the two cases $w_{i_1}(t_0) = 0$ and $w_{i_1}(t_0) \neq 0$ separately.

**Case 1:** $w_{i_1}(t_0) = 0$. In this case, we show that packet $p' + 1$ is routed to the input link of cell $i_1$ at time $t_0$, and packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i_1$ consecutively at time $t_0 + \ell_{i_1} - 1$ and time $t_0 + \ell_{i_1}$, respectively.

As packet $p'$ is the latest arrival packet in the $2k + 1$ cells at time $t_0 - 1$, it is also the latest arrival packet in cell $i_1$ at time $t_0 - 1$. Thus, we see from (10) that packet $p'$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1)$ at time $t_0 - 1$, and hence packet $p'$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1 - j)$ at time $t_0 - 1 + j$ for $j = 0, 1, \ldots, \ell_{i_1} - 1$. In other words, packet $p'$ is stored in cell $i_1$ during the time period $[t_0 - 1, t_0 + \ell_{i_1} - 2]$. Since in this case we have $w_{i_1}(t_0) = 0$, it is clear from (26) that

$$w_{j_1(t_0)}(t_0) = w_{i_1}(t_0) = 0. \quad (27)$$

From (25)–(27), (17), and (16), we see that switch $i$ is set to the “bar” state at time $t_0$ for $i = 0, 1, \ldots, i_1 - 1$ and switch $i_1$ is set to the “cross” state at time $t_0$. Since packet $p' + 1$ is admitted into the network element at time $t_0$, it then follows that packet $p' + 1$ is routed to the input link of cell $i_1$ at time $t_0$ and is also routed into the fiber delay line in cell $i_1$ at time $t_0$ (see Figure 9) so that packet $p' + 1$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1 - j)$ at time $t_0 + j$ for $j = 0, 1, \ldots, \ell_{i_1} - 1$. In other words, packet $p' + 1$ is stored in cell $i_1$ during the time period $[t_0, t_0 + \ell_{i_1} - 1]$. Since cell $i_1$ is nonempty during the time period $[t_0 - 1, t_0 + \ell_{i_1} - 1]$, we can see from (16) that switch $i_1$ is set to the “cross” state during the time period $[t_0, t_0 + \ell_{i_1}]$. Therefore, packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i_1$ consecutively at time $t_0 + \ell_{i_1} - 1$ and time $t_0 + \ell_{i_1}$, respectively.

![Diagram](image-url)

Fig. 9. Packet $p' + 1$ at time $t_0$ in Case 1 in the proof of Lemma 6(i).

**Case 2:** $w_{i_1}(t_0) \neq 0$. In this case, we show that packet $p' + 1$ is routed to the input link of cell $i_1$ at time $t_0 + w_{i_1}(t_0)$, and packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i_1$ consecutively at time $t_0 + w_{i_1}(t_0) - 1$ and time $t_0 + w_{i_1}(t_0)$, respectively.

As packet $p'$ is the latest arrival packet in the $2k + 1$ cells at time $t_0 - 1$, it is also the latest arrival packet in cell $i_1$ at time $t_0 - 1$. Thus, we see from (10) that packet $p'$ is stored in buffer $b_{i_1}(w_{i_1}(t_0) - 1)$ at time $t_0 - 1$, and hence it is stored in buffer $b_{i_1}(j)$ at time $t_0 + w_{i_1}(t_0) - 2 - j$ for $j = 0, 1, \ldots, \ell_{i_1} - 1$. In other words, packet $p'$ is stored in cell $i_1$ during the time period $[t_0 + w_{i_1}(t_0) - \ell_{i_1} - 1, t_0 + w_{i_1}(t_0) - 2]$. 
Let $m(t_0)$ be the number of “1” entries in the $C$-transform $(I_0(w_i(t_0); e_0^{i-1}), I_1(w_i(t_0); e_0^{i-1}), \ldots, I_{i-1}(w_i(t_0); e_0^{i-1}))$ of the virtual waiting time $w_i(t_0)$ of cell $i_1$ at time $t_0$ with respect to the $i_1$-vector $e_0^{i-1} = (e_0, e_1, \ldots, e_{i_1-1})$, say $I_{h_1(t_0)}(w_i(t_0); e_0^{i-1}) = I_{h_2(t_0)}(w_i(t_0); e_0^{i-1}) = \cdots = I_{h_m(t_0)}(w_i(t_0); e_0^{i-1}) = 1$, where $0 \leq h_1(t_0) < h_2(t_0) < \cdots < h_m(t_0) \leq i_1 - 1$. Note from (9) and $e_0^{i-1} \in A_k$ that

$$w_i(t_0) \leq \ell_{i_1} - 1 \leq \sum_{j=0}^{i_1-1} \ell_j.$$  

It then follows from $w_i(t_0) \leq \sum_{j=0}^{i_1-1} \ell_j$, $e_0^{i-1} \subset A_k$, and the unique representation property of $C$-transform in [14] that

$$w_i(t_0) = \sum_{i=0}^{i_1-1} I_i(w_i(t_0); e_0^{i-1}) \ell_i = \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)}.$$  (28)

For convenience, let

$$t_m = t_0 + \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)}, \text{ for } 1 \leq m \leq m(t_0).$$  (29)

We claim that for $1 \leq m \leq m(t_0)$, packet $p' + 1$ is stored in buffer $b_{h_m(t_0)}(0)$ at time $t_m - 1$, cell $i$ is empty during the time period $[t_0, t_m - 1]$ for $h_m(t_0) + 1 \leq i \leq i_1 - 1$, i.e.,

$$g_i(t') = 0, \text{ for } h_m(t_0) + 1 \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_m - 1,$$  (30)

and there are no packets at the output link of cell $i$ during the time period $[t_0, t_m - 1]$ for $h_m(t_0) \leq i \leq i_1 - 1$, i.e.,

$$d_i(t') = 0, \text{ for } h_m(t_0) \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_m - 1.$$  (31)

We show the claim by induction on $m$. From (26) and (28), we have

$$w_{j_1(t_0)}(t_0) = w_i(t_0) = \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)}.$$  (32)

From (25), (32), and (17), we see that switch $i$ is set to the “bar” state at time $t_0$ for $i = 0, 1, \ldots, h_1(t_0) - 1$ and switch $h_1(t_0)$ is set to the “cross” state at time $t_0$. Since packet $p' + 1$ is admitted into the network element at time $t_0$, it is clear that packet $p' + 1$ is routed into the fiber delay line in cell $h_1(t_0)$ at time $t_0$, and hence packet $p' + 1$ is stored in buffer $b_{h_1(t_0)}(t_0 + \ell_{h_1(t_0)} - 1 - j)$ at time $t_0 + j$ for $j = 0, 1, \ldots, \ell_{h_1(t_0)} - 1$. In particular, packet $p' + 1$ is stored in buffer $b_{h_1(t_0)}(0)$ at time $t_0 + \ell_{h_1(t_0)} - 1 = t_1 - 1$, where we have used $t_1 = t_0 + \ell_{h_1(t_0)}$ in (29).

As it is clear that packet $p' + 1$ is stored in cell $h_1(t_0)$ during the time period $[t_0, t_1 - 1]$, we see from (16) that switch $h_1(t_0)$ is set to the “cross” state during the time period $[t_0 + 1, t_1]$. Since we have already shown that switch $h_1(t_0)$ is set to the “cross” state at time $t_0$, it follows that
switch \( h_1(t_0) \) is set to the “cross” state during the time period \([t_0, t_1]\). As \( 0 \leq h_1(t_0) \leq i_1 - 1 \), it is immediate from (23) that \( q_{h_1(t_0)}(t_0 - 1) = 0 \), i.e., cell \( h_1(t_0) \) is empty at time \( t_0 - 1 \), and hence it is easy to deduce that buffer \( b_{h_1(t_0)}(0) \) is empty during the time period \([t_0 - 1, t_1 - 2]\) (note that the length of this time period is \( t_1 - t_0 = \ell_{h_1(t_0)} \), which is equal to the length of the fiber delay line in cell \( h_1(t_0) \)). Since we know that switch \( h_1(t_0) \) is set to the “cross” state during the time period \([t_0, t_1 - 1]\), it then follows that there are no packets at the output link of cell \( h_1(t_0) \) during the time period \([t_0, t_1 - 1]\) and we have

\[
d_{h_1(t_0)}(t') = 0, \quad \text{for} \quad t_0 \leq t' \leq t_1 - 1. \tag{33}
\]

We are now ready to show that (30) and (31) hold for \( m = 1 \). For \( h_1(t_0) + 1 \leq i' \leq i_1 - 1 \) and \( t_0 \leq t' \leq t_1 - 1 \), we have from (22), \( a_i(t'') = d_{i-1}(t'') \) for all \( 1 \leq i \leq 2k \) and \( t'' \geq 0 \), (23), and (33) that

\[
\sum_{i=h_1(t_0)+1}^{i'} q_i(t') = \sum_{i=h_1(t_0)+1}^{i'} (q_i(t' - 1) + a_i(t') - d_i(t'))
\]

\[
= \sum_{i=h_1(t_0)+1}^{i'} ((q_i(t' - 2) + a_i(t' - 1) - d_i(t' - 1)) + a_i(t') - d_i(t'))
\]

\[
= \sum_{i=h_1(t_0)+1}^{i'} \left( q_i(t_0 - 1) + \sum_{t''=t_0}^{t'} (a_i(t'') - d_i(t'')) \right)
\]

\[
= \sum_{i=h_1(t_0)+1}^{i'} q_i(t_0 - 1) + \sum_{t''=t_0}^{t'} \sum_{i=h_1(t_0)+1}^{i'} (a_i(t'') - d_i(t''))
\]

\[
= \sum_{i=h_1(t_0)+1}^{i'} q_i(t_0 - 1) + \sum_{t''=t_0}^{t'} \sum_{i=h_1(t_0)+1}^{i'} (d_{i-1}(t'') - d_i(t''))
\]

\[
= \sum_{i=h_1(t_0)+1}^{i'} q_i(t_0 - 1) + \sum_{t''=t_0}^{t'} (d_{h_1(t_0)}(t'') - d_i(t''))
\]

\[
= - \sum_{t''=t_0}^{t'} d_{i'}(t''). \tag{34}
\]

We can write (34) as

\[
\sum_{i=h_1(t_0)+1}^{i'} q_i(t') + \sum_{t''=t_0}^{t'} d_{i'}(t'') = 0, \quad \text{for} \quad h_1(t_0) + 1 \leq i' \leq i_1 - 1 \quad \text{and} \quad t_0 \leq t' \leq t_1 - 1. \tag{35}
\]
It then follows from (33), (35), and the nonnegativity of \( q_i(t') \) and \( d'_i(t'') \) that

\[
q_i(t') = 0, \quad \text{for } h_1(t_0) + 1 \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_1 - 1, \tag{36}
\]

\[
d'_i(t') = 0, \quad \text{for } h_1(t_0) \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_1 - 1. \tag{37}
\]

Therefore, the claim holds for \( m = 1 \).

Assume as the induction hypothesis that the claim holds for some \( 1 \leq m \leq m(t_0) - 1 \). From (9), we see that \( w_{i_1}(t_0) \leq \ell_{i_1} - 1 \) and hence we have

\[
(t_0 - 1) - (t_0 + w_{i_1}(t_0) - \ell_{i_1} - 1) = \ell_{i_1} - w_{i_1}(t_0) > 0. \tag{38}
\]

From (29), \( m \geq 1 \), and \( h_1(t_0) \geq 0 \), we have

\[
(t_m - 1) - (t_0 - 1) = \sum_{j=1}^{m} \ell_{h_j(t_0)} \geq \ell_{h_1(t_0)} > 0. \tag{39}
\]

From (28), (29), \( 1 \leq m \leq m(t_0) - 1 \), and \( h_{m+1}(t_0) \geq h_2(t_0) \geq 1 \), we have

\[
(t_0 + w_{i_1}(t_0) - 2) - (t_m - 1) = \left( t_0 + \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)} - 2 \right) - \left( t_0 + \sum_{j=1}^{m} \ell_{h_j(t_0)} - 1 \right)
= \sum_{j=m+1}^{m(t_0)} \ell_{h_j(t_0)} - 1 \geq \ell_{h_{m+1}(t_0)} - 1 > 0. \tag{40}
\]

Thus, we see from (38)–(40) that

\[
t_0 + w_{i_1}(t_0) - \ell_{i_1} - 1 < t_0 - 1 < t_m - 1 < t_0 + w_{i_1}(t_0) - 2. \tag{41}
\]

As packet \( p' \) is stored in cell \( i_1 \) during the time period \([t_0 + w_{i_1}(t_0) - \ell_{i_1} - 1, t_0 + w_{i_1}(t_0) - 2]\), it follows from (41) that packet \( p' \) is stored in cell \( i_1 \) during the time period \([t_0 - 1, t_m - 1]\).

As packet \( p' \) is stored in cell \( i_1 \) during the time period \([t_0 - 1, t_m - 1]\), we see from (16) that switch \( i_1 \) is set to the “cross” state during the time period \([t_0, t_m]\). From the induction hypothesis, we know that there are no packets at the output link of cell \( i_1 - 1 \), i.e., there are no packets at the input link of cell \( i_1 \), during the time period \([t_0, t_m - 1]\), and hence it is easy to see that there are no packets routed to the fiber delay line in cell \( i_1 \) during the time period \([t_0, t_m - 1]\).

Since packet \( p' \) is the latest arrival packet in cell \( i_1 \) at time \( t_0 - 1 \), it then follows that packet \( p' \) remains the latest arrival packet in cell \( i_1 \) during the time period \([t_0, t_m - 1]\). As we know that packet \( p' \) is stored in buffer \( b_{i_1}(j) \) at time \( t_0 + w_{i_1}(t_0) - 2 - j \) for \( j = 0, 1, \ldots, \ell_{i_1} - 1 \), we see from \( t_0 + w_{i_1}(t_0) - \ell_{i_1} - 1 < t_m - 1 < t_0 + w_{i_1}(t_0) - 2 \) in (41) that packet \( p' \) is stored in buffer \( b_{i_1}(t_0 + w_{i_1}(t_0) - t_m - 1) \) at time \( t_m - 1 \). As such, we have from (9), \( t_0 + w_{i_1}(t_0) - t_m - 1 < \ell_{i_1} - 1 \) in (41), (28), and (29) that

\[
w_{i_1}(t_m) = (t_0 + w_{i_1}(t_0) - t_m - 1) + 1 = \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)} - \sum_{j=1}^{m} \ell_{h_j(t_0)} = \sum_{j=m+1}^{m(t_0)} \ell_{h_j(t_0)}. \tag{42}
\]
As packet \( p' \) is stored in cell \( i_1 \) at time \( t_m - 1 \) and we have from the induction hypothesis that packet \( p' + 1 \) is stored in buffer \( b_{h_m(t_0)}(0) \) at time \( t_m - 1 \), it is clear that

\[
q_{h_m(t_0)}(t_m - 1) \neq 0 \quad \text{and} \quad q_{i_1}(t_m - 1) \neq 0.
\] (43)

Furthermore, we have from the induction hypothesis that

\[
q_i(t_m - 1) = 0, \quad \text{for} \quad h_m(t_0) + 1 < i \leq i_1 - 1.
\] (44)

From (8), \( 0 \leq h_m(t_0) < i_1 \leq k - 1 \), and (43), we have

\[
q^{(1)}(t_m - 1) = \sum_{i=0}^{k-1} q_i(t_m - 1) \neq 0.
\] (45)

From (43) and (44), we can see that

\[
j_{n-1}(t_m) = h_m(t_0) \quad \text{and} \quad j_n(t_m) = i_1, \quad \text{for some} \quad 2 \leq n \leq n(t_m),
\] (46)

where \( n(t_m) \) is the number of nonempty cells among the first \( k \) cells at time \( t_m - 1 \) and \( j_{n-1}(t_m) \) and \( j_n(t_m) \) are the indices of the \( (n-1)^{th} \) nonempty cell and the \( n^{th} \) nonempty cell, respectively, among the first \( k \) cells at time \( t_m - 1 \) as defined in (C2). From (46) and (42), we have

\[
w_{j_n(t_m)}(t_m) = w_{i_1}(t_m) = \sum_{j=m+1}^{m(t_0)} \ell_{h_j(t_0)}.
\] (47)

Thus, we have for \( i = 0, 1, \ldots, i_1 - 1 \),

\[
I_i(w_{j_n(t_m)}(t_m); \ell_0^{i_1-1}) = \begin{cases} 
1, & \text{if} \quad i = h_{m+1}(t_0), h_{m+2}(t_0), \ldots, h_{m(t_0)}(t_0), \\
0, & \text{otherwise},
\end{cases}
\] (48)

in the \( C \)-transform \((I_0(w_{j_n(t_m)}(t_m); \ell_0^{i_1-1}), I_1(w_{j_n(t_m)}(t_m); \ell_0^{i_1-1}), \ldots, I_{k-1}(w_{j_n(t_m)}(t_m); \ell_0^{i_1-1}))\) of the virtual waiting time \( w_{j_n(t_m)}(t_m) \) of cell \( j_n(t_m) \) at time \( t_m \) with respect to the \( i_1 \)-vector \( \ell_0^{i_1-1} = (\ell_0, \ell_1, \ldots, \ell_{i_1-1}) \).

From (45)–(47), (48), (16), and (17), we see that switch \( h_m(t_0) \) and switch \( h_{m+1}(t_0) \) are set to the “cross” state at time \( t_m \) and switch \( i \) is set to the “bar” state at time \( t_m \) for \( i = h_m(t_0) + 1, h_m(t_0) + 2, \ldots, h_{m+1}(t_0) - 1 \). Since we have from the induction hypothesis that packet \( p' + 1 \) is stored in buffer \( b_{h_m(t_0)}(0) \) at time \( t_m - 1 \), it then follows that packet \( p' + 1 \) is routed into the fiber delay line in cell \( h_{m+1}(t_0) \) at time \( t_m \) (see Figure 10), and hence packet \( p' + 1 \) is stored in buffer \( b_{h_{m+1}(t_0)}(\ell_{h_{m+1}(t_0)} - 1 - j) \) at time \( t_m + j \) for \( j = 0, 1, \ldots, \ell_{h_{m+1}(t_0)} - 1 \). In particular, packet \( p' + 1 \) is stored in buffer \( b_{h_{m+1}(t_0)}(0) \) at time \( t_m + \ell_{h_{m+1}(t_0)} - 1 = t_m + \ell_{h_{m+1}(t_0)} - 1 = t_0 + \sum_{j=1}^{m} \ell_{h_j(t_0)} + \ell_{h_{m+1}(t_0)} - 1 = t_m + 1 - 1 \), where we have used (29) in the second and the third equalities.

As it is clear that packet \( p' + 1 \) is stored in cell \( h_{m+1}(t_0) \) during the time period \([t_m, t_{m+1} - 1]\), we see from (16) that switch \( h_{m+1}(t_0) \) is set to the “cross” state during the time period \([t_m + 1, t_{m+1}]\).
follows that switch \( h_m(t_0) \) is set to the “cross” state at time \( t_m \), it follows that switch \( h_m(t_0) \) is set to the “cross” state during the time period \([t_m, t_{m+1}]\). As \( h_m(t_0) < h_{m+1}(t_0) \leq i_1 - 1 \), it is immediate from (44) that \( q_{h_m(t_0)}(t_m - 1) = 0 \), i.e., cell \( h_{m+1}(t_0) \) is empty at time \( t_m - 1 \), and hence it is easy to deduce that buffer \( b_{h_{m+1}(t_0)}(0) \) is empty during the time period \([t_m - 1, t_{m+1} - 2]\) (note that the length of this time period is \( t_{m+1} - t_m = \ell_{h_{m+1}(t_0)} \), which is equal to the length of the fiber delay line in cell \( h_{m+1}(t_0) \)). Since we know that switch \( h_{m+1}(t_0) \) is set to the “cross” state during the time period \([t_m, t_{m+1} - 1]\), we then see that there are no packets at the output link of cell \( h_{m+1}(t_0) \) during the time period \([t_m, t_{m+1} - 1]\) and we have

\[
d_{h_{m+1}(t_0)}(t') = 0, \quad \text{for } t_m \leq t' \leq t_{m+1} - 1. \tag{49}
\]

We are now ready to show that (30) and (31) hold with \( m \) replaced by \( m + 1 \). For \( h_{m+1}(t_0) + 1 \leq i' \leq i_1 - 1 \) and \( t_m \leq t' \leq t_{m+1} - 1 \), we have from (22), \( a_i(t'') = d_{i-1}(t'') \) for all \( 1 \leq i \leq 2k \) and \( t'' \geq 0 \), (44), and (49) that

\[
\sum_{i=h_{m+1}(t_0)+1}^{i'} q_i(t') = \sum_{i=h_{m+1}(t_0)+1}^{i'} \left( q_i(t_m - 1) + \sum_{t''=t_m}^{t'} (a_i(t'') - d_i(t'')) \right)
\]

\[
= \sum_{i=h_{m+1}(t_0)+1}^{i'} q_i(t_m - 1) + \sum_{t''=t_m}^{t'} \sum_{i=h_{m+1}(t_0)+1}^{i'} (a_i(t'') - d_i(t''))
\]

\[
= \sum_{i=h_{m+1}(t_0)+1}^{i'} q_i(t_m - 1) + \sum_{t''=t_m}^{t'} \sum_{i=h_{m+1}(t_0)+1}^{i'} (d_{i-1}(t'') - d_i(t''))
\]

\[
= \sum_{i=h_{m+1}(t_0)+1}^{i'} q_i(t_m - 1) + \sum_{t''=t_m}^{t'} (d_{h_{m+1}(t_0)}(t'') - d_i(t''))
\]

\[
= - \sum_{t''=t_m}^{t'} d_i(t''). \tag{50}
\]

Fig. 10. Packet \( p' + 1 \) at time \( t_m \) in Case 2 in the proof of Lemma 6(i).
We can write (50) as
\[ \sum_{i=h_{m+1}(t_0)+1}^{t'} q_i(t') + \sum_{t''=t_m}^{t'} d_i(t'') = 0, \text{ for } h_{m+1}(t_0)+1 \leq i' \leq i_1 - 1 \text{ and } t_m \leq t' \leq t_{m+1} - 1. \tag{51} \]

It then follows from (49), (51), and the nonnegativity of \( q_i(t') \) and \( d_i(t'') \) that
\[
q_i(t') = 0, \text{ for } h_{m+1}(t_0)+1 \leq i \leq i_1 - 1 \text{ and } t_m \leq t' \leq t_{m+1} - 1, \tag{52}
\]
\[
d_i(t') = 0, \text{ for } h_{m+1}(t_0) \leq i \leq i_1 - 1 \text{ and } t_m \leq t' \leq t_{m+1} - 1. \tag{53}
\]

From the induction hypothesis and \( 0 \leq h_m(t_0) < h_{m+1}(t_0) \leq i_1 - 1 \), we have
\[
q_i(t') = 0, \text{ for } h_{m+1}(t_0)+1 \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_m - 1, \tag{54}
\]
\[
d_i(t') = 0, \text{ for } h_{m+1}(t_0) \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_m - 1. \tag{55}
\]

By combining (52)–(55), we obtain
\[
q_i(t') = 0, \text{ for } h_{m+1}(t_0)+1 \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_{m+1} - 1, \tag{56}
\]
\[
d_i(t') = 0, \text{ for } h_{m+1}(t_0) \leq i \leq i_1 - 1 \text{ and } t_0 \leq t' \leq t_{m+1} - 1. \tag{57}
\]

Therefore, the claim holds for \( m + 1 \) and the induction is completed.

Note that from (29) and (28), we have
\[ t_{m(t_0)} - 1 = t_0 + \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)} - 1 = t_0 + w_{i_1}(t_0) - 1. \tag{58} \]

From the claim shown above and (58), we know that packet \( p' + 1 \) is stored in buffer \( b_{h_{m(t_0)}(t_0)}(0) \) at time \( t_{m(t_0)} - 1 = t_0 + w_{i_1}(t_0) - 1 \), and hence we have
\[ q_{h_{m(t_0)}(t_0)}(t_0 + w_{i_1}(t_0) - 1) \neq 0. \tag{59} \]

It follows from (8), \( 0 \leq h_{m(t_0)}(t_0) \leq i_1 - 1 < k - 1 \), and (59) that
\[ q^{(1)}(t_0 + w_{i_1}(t_0) - 1) = \sum_{i=0}^{k-1} q_i(t_0 + w_{i_1}(t_0) - 1) \neq 0. \tag{60} \]

Since packet \( p' \) is stored in buffer \( b_{i_1}(0) \) at time \( t_0 + w_{i_1}(t_0) - 2 \), we see from (16) that switch \( i_1 \) is set to the “cross” state at time \( t_0 + w_{i_1}(t_0) - 1 \), and hence packet \( p' \) is routed to the output link of cell \( i_1 \) at time \( t_0 + w_{i_1}(t_0) - 1 \). It remains to show that packet \( p' + 1 \) is routed to the input link and the output link of cell \( i_1 \) at time \( t_0 + w_{i_1}(t_0) \). We need to consider the following two subcases.

Subcase 2(a): Packet \( p' \) is routed into the fiber delay line in cell \( i_2 \) at time \( t_0 + w_{i_1}(t_0) - 1 \) for some \( i_1 + 1 \leq i_2 \leq k - 1 \) (see Figure 11(a)).
In this subcase, it is clear that packet $p'$ is stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t_0 + w_{i_1}(t_0) - 1$, and hence we have

$$q_{i_2}(t_0 + w_{i_1}(t_0) - 1) \neq 0. \quad (61)$$

Since packet $p'$ is stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t_0 + w_{i_1}(t_0) - 1$, packet $p' + 1$ is stored in buffer $b_{h_{m(t_0)}(t_0)}(0)$ at time $t_0 + w_{i_1}(t_0) - 1$, $0 \leq h_{m(t_0)}(t_0) \leq i_1 - 1 < i_2 \leq k - 1$, and we know from Lemma 5(ii) that packets stored in the first $k$ cells satisfy the ordered property in (A2) at all times and packets stored in any one of the first $k$ cells at any time are ordered according to their arrival times, we immediately see that

$$q_i(t_0 + w_{i_1}(t_0) - 1) = 0, \text{ for } h_{m(t_0)}(t_0) + 1 \leq i \leq i_2 - 1, \quad (62)$$

and packet $p'$ is the latest arrival packet in cell $i_2$ at time $t_0 + w_{i_1}(t_0) - 1$, and hence we see from (9) that

$$w_{i_2}(t_0 + w_{i_1}(t_0)) = 0. \quad (63)$$

From (59), (61), and (62), we can see that

$$j_{n-1}(t_0 + w_{i_1}(t_0)) = h_{m(t_0)}(t_0) \quad \text{and} \quad j_n(t_0 + w_{i_1}(t_0)) = i_2, \text{ for some } 2 \leq n \leq n(t_0 + w_{i_1}(t_0)), \quad (64)$$

where $n(t_0 + w_{i_1}(t_0))$ is the number of nonempty cells among the first $k$ cells at time $t_0 + w_{i_1}(t_0) - 1$ and $j_{n-1}(t_0 + w_{i_1}(t_0))$ and $j_n(t_0 + w_{i_1}(t_0))$ are the indices of the $(n-1)^{\text{th}}$ nonempty cell and the $n^{\text{th}}$ nonempty cell, respectively, among the first $k$ cells at time $t_0 + w_{i_1}(t_0) - 1$ as defined in (C2).
From (64) and (63), we have
\[ w_{j_0(t_0+w_{i_1}(t_0))}(t_0 + w_{i_1}(t_0)) = w_{i_2}(t_0 + w_{i_1}(t_0)) = 0. \] (65)

From (60), (64), (65), (16), and (17), we see that switch \( h_{m(t_0)}(t_0) \) and switch \( i_2 \) are set to the “cross” state at time \( t_0 + w_{i_1}(t_0) \) and switch \( i \) is set to the “bar” state at time \( t_0 + w_{i_1}(t_0) \) for \( i = h_{m(t_0)}(t_0) + 1, h_{m(t_0)}(t_0) + 2, \ldots, i_2 - 1 \). Since packet \( p' + 1 \) is stored in buffer \( b_{h_{m(t_0)}(t_0)}(0) \) at time \( t_0 + w_{i_1}(t_0) - 1 \) and \( h_{m(t_0)}(t_0) + 1 \leq i_1 \leq i_2 - 1 \), it then follows that packet \( p' + 1 \) is routed to the input link and the output link of cell \( i_1 \) at time \( t_0 + w_{i_1}(t_0) \) (see Figure 11(b)).

**Subcase 2(b):** Packet \( p' \) is routed to the output link of cell \( k - 1 \) at time \( t_0 + w_{i_1}(t_0) - 1 \) (see Figure 12(a)).

![Fig. 12](image)

As packet \( p' \) is stored in buffer \( b_{i_1}(0) \) at time \( t_0 + w_{i_1}(t_0) - 2 \) and in this subcase it is routed to the output link of cell \( k - 1 \) at time \( t_0 + w_{i_1}(t_0) - 1 \), we see from Lemma 5(iii) that packet \( p' \) is the earliest arrival packet in the first \( k \) cells at time \( t_0 + w_{i_1}(t_0) - 2 \). Since packet \( p' \) is routed to the output link of cell \( k - 1 \) at time \( t_0 + w_{i_1}(t_0) - 1 \) (so that it is not stored in the first \( k \) cells at time \( t_0 + w_{i_1}(t_0) - 1 \)) and we know that packet \( p' + 1 \) is stored in buffer \( b_{h_{m(t_0)}(t_0)}(0) \) at time \( t_0 + w_{i_1}(t_0) - 1 \), it is clear that packet \( p' + 1 \) is the earliest arrival packet in the first \( k \) cells at time \( t_0 + w_{i_1}(t_0) - 1 \). Furthermore, as \( 0 \leq h_{m(t_0)}(t_0) \leq i_1 - 1 < k - 1 \) and we know from Lemma 5(ii) that packets stored in the first \( k \) cells satisfy the ordered property in (A2) at all times, it then follows that
\[ q_i(t_0 + w_{i_1}(t_0) - 1) = 0, \text{ for } h_{m(t_0)}(t_0) + 1 \leq i \leq k - 1. \] (66)
From (59) and (66), we can see that
\[ j_{n(t_0 + w_i(t_0))}(t_0 + w_i(t_0)) = h_{m(t_0)}(t_0), \]  
(67)
where \( n(t_0 + w_i(t_0)) \) is the number of nonempty cells among the first \( k \) cells at time \( t_0 + w_i(t_0) - 1 \) and \( j_{n(t_0 + w_i(t_0))} \) is the largest index of a nonempty cell among the first \( k \) cells at time \( t_0 + w_i(t_0) - 1 \) as defined in (C2).

As packet \( p' \) is routed to the output link of cell \( k - 1 \) at time \( t_0 + w_i(t_0) - 1 \) in this subcase, we have
\[ d_{k-1}(t_0 + w_i(t_0) - 1) = 1. \]  
(68)
From (60), (67), (68), (16), and (18), we see that switch \( h_{m(t_0)}(t_0) \) is set to the “cross” state at time \( t_0 + w_i(t_0) \) and switch \( i \) is set to the “bar” state at time \( t_0 + w_i(t_0) \) for \( i = h_{m(t_0)}(t_0) + 1, h_{m(t_0)}(t_0) + 2, \ldots, k - 1 \). Since packet \( p' + 1 \) is stored in buffer \( b_{h_{m(t_0)}(t_0)}(0) \) at time \( t_0 + w_i(t_0) - 1 \) and \( h_{m(t_0)}(t_0) + 1 \leq i_1 \leq k - 1 \), it then follows that packet \( p' + 1 \) is routed to the input link and the output link of cell \( i_1 \) at time \( t_0 + w_i(t_0) \) (see Figure 12(b)).

(ii) Note that (23) and (24) still hold in this case. As in this case we have \( k \leq i_1 \leq 2k \), it follows from (8), (23), and (24) that
\[ q^{(1)}(t_0 - 1) = \sum_{i=0}^{k-1} q_i(t_0 - 1) = 0 \quad \text{and} \quad q^{(2)}(t_0 - 1) = \sum_{i=k}^{2k} q_i(t_0 - 1) \neq 0, \]  
(69)
and the smallest index \( j(t_0) \) of a nonempty cell among the last \( k + 1 \) cells at time \( t_0 - 1 \) as defined in (14) is given by
\[ j(t_0) = i_1. \]  
(70)
We then consider the two cases \( w_i(t_0) = 0 \) and \( w_i(t_0) \neq 0 \) separately.

Case 1: \( w_i(t_0) = 0 \). From (70) and \( w_i(t_0) = 0 \) in this case, we have
\[ w_{j(t_0)}(t_0) = w_i(t_0) = 0. \]  
(71)
From (69), (71), and (15) we see that switch \( i \) is set to the “bar” state at time \( t_0 \) for \( i = 0, 1, \ldots, k - 1 \). As packet \( p' + 1 \) is admitted into the network element at time \( t_0 \), it is easy to see that packet \( p' + 1 \) is routed to the output link of cell \( k - 1 \) at time \( t_0 = t_0 + w_i(t_0) \).

Case 2: \( w_i(t_0) \neq 0 \). Let \( m(t_0) \) be the number of “1” entries in the \( C \)-transform \((I_0(w_i(t_0)); \ell_0^{k-1}), I_1(w_i(t_0); \ell_1^{k-1}), \ldots, I_{k-1}(w_i(t_0); \ell_{k-1}^{k-1})\) of the virtual waiting time \( w_i(t_0) \) of cell \( i_1 \) at time \( t_0 \) with respect to the \( k \)-vector \( \ell_0^{k-1} = (\ell_0, \ell_1, \ldots, \ell_{k-1}) \), say \( I_{h_1(t_0)}(w_i(t_0); \ell_0^{k-1}) = I_{h_2(t_0)}(w_i(t_0); \ell_1^{k-1}) = \cdots = I_{h_{m(t_0)}(t_0)}(w_i(t_0); \ell_{k-1}^{k-1}) = 1 \), where \( 0 \leq h_1(t_0) < h_2(t_0) < \cdots < h_{m(t_0)}(t_0) \leq k - 1 \). Note from (9), (4), and (2) that
\[ w_i(t_0) \leq \ell_{i_1} - 1 \leq \ell_k - 1 \leq \sum_{j=0}^{k-1} \ell_j. \]
It then follows from $w_i(t_o) \leq \sum_{j=0}^{k-1} \ell_j$, $\ell_0^{k-1} \in A_k$, and the unique representation property of $C$-transform in [14] that

$$w_i(t_o) = \sum_{i=0}^{k-1} I_i(w_i(t_o); \ell_0^{i-1}) \ell_i = \sum_{j=1}^{m(t_o)} \ell_{j(t_o)}.$$  \hfill (72)

Let $t_m = t_o + \sum_{j=1}^{m} \ell_{j(t_o)}$ for $1 \leq m \leq m(t_o)$ as in (29). We claim that for $1 \leq m \leq m(t_o)$, packet $p' + 1$ is stored in buffer $b_{m(t_o)}(0)$ at time $t_m - 1$, cell $i$ is empty during the time period $[t_0, t_m - 1]$ for $h_m(t_o) + 1 \leq i \leq i_1 - 1$, i.e., (30) holds, there are no packets at the output link of cell $i$ during the time period $[t_0, t_m - 1]$ for $h_m(t_o) \leq i \leq i_1 - 1$, i.e., (31) holds, and the connection pattern of switch $i$ is the same during the time period $[t_0, t_m]$ for $h_m(t_o) + 1 \leq i \leq k - 1$.

We show the claim by induction on $m$. From (70) and (72), we have

$$w_{j(t_o)}(t_o) = w_i(t_o) = \sum_{j=1}^{m(t_o)} \ell_{j(t_o)}.$$  \hfill (73)

From (69), (73), and (15), we see that switch $i$ is set to the “cross” state at time $t_0$ for $i = h_1(t_0), h_2(t_0), \ldots, h_{m(t_o)}(t_o)$, and is set to the “bar” state at time $t_0$ for $0 \leq i \leq k - 1$ with $i \neq h_1(t_0), h_2(t_0), \ldots, h_{m(t_o)}(t_o)$. Since packet $p' + 1$ is admitted into the network element at time $t_0$, it then follows that packet $p' + 1$ is routed into the fiber delay line in cell $h_1(t_0)$ at time $t_0$, and hence packet $p' + 1$ is stored in buffer $b_{h_1(t_0)}(0)$ at time $t_0 + \ell_{h_1(t_0)} - 1 = t_1 - 1$, where we have used $t_1 = t_0 + \ell_{h_1(t_0)}$ in (29). By using the same argument as in Case 2 in the proof of Lemma 6(i), we can show that (33)–(37) still hold, and we immediately see from (36) and (37) that (30) and (31) hold for $m = 1$.

As it is clear that packet $p' + 1$ is stored in cell $h_1(t_0)$ during the time period $[t_0, t_1 - 1]$, we have

$$q_{h_1(t_o)}(t') \neq 0, \text{ for } t_0 \leq t' \leq t_1 - 1.$$  \hfill (74)

From (8), $0 \leq h_1(t_0) \leq k - 1$, and (74), we have

$$q^{(1)}(t') = \sum_{i=0}^{k-1} q_i(t') \neq 0, \text{ for } t_0 \leq t' \leq t_1 - 1.$$  \hfill (75)

From (74), (36), and $h_1(t_0) \leq k - 1 \leq i_1 - 1$, we can see that

$$j_{n(t'+1)}(t' + 1) = h_1(t_0), \text{ for } t_0 \leq t' \leq t_1 - 1,$$  \hfill (76)

where $n(t'+1)$ is the number of nonempty cells among the first $k$ cells at time $t'$ and $j_{n(t'+1)}(t'+1)$ is the largest index of a nonempty cell among the first $k$ cells at time $t'$. From (37) and $h_1(t_0) \leq k - 1 \leq i_1 - 1$, we also have

$$d_{k-1}(t') = 0, \text{ for } t_0 \leq t' \leq t_1 - 1.$$  \hfill (77)
Thus, it follows from (75)–(77) and (18) that \(c_i(t' + 1) = c_i(t')\) for \(h_1(t_0) + 1 \leq i \leq k - 1\) and \(t_0 \leq t' \leq t_1 - 1\), namely, the connection pattern of switch \(i\) is the same during the time period \([t_0, t_1]\) for \(h_1(t_0) + 1 \leq i \leq k - 1\). Therefore, we have shown that the claim holds for \(m = 1\).

Assume as the induction hypothesis that the claim holds for some \(1 \leq m \leq m(t_0) - 1\). Since we have from the induction hypothesis that packet \(p' + 1\) is stored in buffer \(b_{h_m(t_0)}(0)\) at time \(t_m - 1\), we see from (16) that switch \(h_m(t_0)\) is set to the “cross” state at time \(t_m\). Since we also have from the induction hypothesis that the connection pattern of switch \(i\) at time \(t_m\) is the same that of switch \(i\) at time \(t_0\) for \(h_m(t_0) + 1 \leq i \leq k - 1\) and we have \(h_m(t_0) + 1 \leq h_{m+1}(t_0) \leq h_m(t_0) \leq k - 1\), we immediately see from the connection patterns of the first \(k\) switches at time \(t_0\) as mentioned after (73) that switch \(i\) is set to the “bar” state at time \(t_m\) for \(i = h_m(t_0) + 1, h_m(t_0) + 2, \ldots, h_{m+1}(t_0) - 1\) and switch \(h_{m+1}(t_0)\) is set to the “cross” state at time \(t_m\). As such, it then follows that packet \(p' + 1\) is routed into the fiber delay line in cell \(h_{m+1}(t_0)\) at time \(t_m\), and hence packet \(p' + 1\) is stored in buffer \(b_{h_{m+1}(t_0)}(0)\) at time \(t_m + \ell_{h_{m+1}(t_0)} - 1 = t_0 + \sum_{j=1}^{m} \ell_{h_j}(t_0) + \ell_{h_{m+1}(t_0)} - 1 = t_{m+1} - 1\), where we have used (29) in the second and the third equalities. By using the same argument as in Case 2 in the proof of Lemma 6(i), we can show that (49)–(57) still hold, and we see from (56) and (57) that (30) and (31) hold for \(m + 1\).

As it is clear that packet \(p' + 1\) is stored in cell \(h_{m+1}(t_0)\) during the time period \([t_m, t_{m+1} - 1]\), we have

\[q_{h_{m+1}(t_0)}(t') \neq 0, \text{ for } t_m \leq t' \leq t_{m+1} - 1.\]  

(78)

From (8), \(0 \leq h_{m+1}(t_0) \leq k - 1\), and (78), we have

\[q^{(1)}(t') = \sum_{i=0}^{k-1} q_i(t') \neq 0, \text{ for } t_m \leq t' \leq t_{m+1} - 1.\]  

(79)

From (78), (56), and \(h_{m+1}(t_0) \leq k - 1 \leq i_1 - 1\), we can see that

\[j_{n(t'+1)}(t'+1) = h_{m+1}(t_0), \text{ for } t_m \leq t' \leq t_{m+1} - 1,\]  

(80)

where \(n(t'+1)\) is the number of nonempty cells among the first \(k\) cells at time \(t'\) and \(j_{n(t'+1)}(t'+1)\) is the largest index of a nonempty cell among the first \(k\) cells at time \(t'\). From (57) and \(h_{m+1}(t_0) \leq k - 1 \leq i_1 - 1\), we also have

\[d_{k-1}(t') = 0, \text{ for } t_m \leq t' \leq t_{m+1} - 1.\]  

(81)

Thus, it follows from (79)–(81) and (18) that \(c_i(t' + 1) = c_i(t')\) for \(h_{m+1}(t_0) + 1 \leq i \leq k - 1\) and \(t_m \leq t' \leq t_{m+1} - 1\), namely, the connection pattern of switch \(i\) is the same during the time period \([t_m, t_{m+1}]\) for \(h_{m+1}(t_0) + 1 \leq i \leq k - 1\). Since we also have from the induction hypothesis and \(h_m(t_0) < h_{m+1}(t_0) \leq h_m(t_0) \leq k - 1\) that the connection pattern of switch \(i\) at time \(t_m\) is the same during the time period \([t_0, t_m]\) for \(h_{m+1}(t_0) + 1 \leq i \leq k - 1\), we immediately
see that the connection pattern of switch \( i \) is the same during the time period \( [t_0, t_{m+1}] \) for \( h_{m+1}(t_0) + 1 \leq i \leq k - 1 \). Therefore, we have shown that the claim holds for \( m + 1 \).

Since we have from the claim shown above that packet \( p' + 1 \) is stored in buffer \( b_{h_{m(t_0)}}(t_0)(0) \) at time \( t_{m(t_0)} - 1 \), we see from (16) that switch \( h_{m(t_0)}(t_0) \) is set to the “cross” state at time \( t_{m(t_0)} \). Since we also have from the claim shown above that the connection pattern of switch \( i \) at time \( t_{m(t_0)} \) is the same that of switch \( i \) at time \( t_0 \) for \( h_{m(t_0)}(t_0) + 1 \leq i \leq k - 1 \), we immediately see from the connection patterns of the first \( k \) switches at time \( t_0 \) as mentioned after (73) that switch \( i \) is set to the “bar” state at time \( t_{m(t_0)} \) for \( i = h_{m(t_0)}(t_0) + 1, h_{m(t_0)}(t_0) + 2, \ldots, k - 1 \). As such, it then follows that packet \( p' + 1 \) is routed to the output link of cell \( k - 1 \) at time \( t_{m(t_0)} \), and we have proved Lemma 6(ii) by observing from (29) and (72) that \( t_{m(t_0)} = t_0 + \sum_{j=1}^{m(t_0)} \ell_{h_j(t_0)} = t_0 + w_{i_1}(t_0) \).

(iii) We consider the two cases “packet \( p' \) is stored in the first \( k \) cells at time \( t - 1 \)” and “packet \( p' \) is not stored in the first \( k \) cells at time \( t - 1 \)” separately.

Case 1: Packet \( p' \) is stored in the first \( k \) cells at time \( t - 1 \), say packet \( p' \) is stored in cell \( i_2 \) at time \( t - 1 \) for some \( i_1 \leq i_2 \leq k - 1 \) (note that \( t_0 \leq t \)). If \( i_2 = i_1 \), then there is nothing to prove. On the other hand, if \( i_1 < i_2 \leq k - 1 \), then we show by induction on \( i \) that packet \( p' \) and packet \( p' + 1 \) are routed to the output link of cell \( i \) consecutively at or before time \( t \) for \( i = i_1, i_1 + 1, \ldots, i_2 - 1 \).

From Lemma 6(i), we know that packet \( p' \) and packet \( p' + 1 \) are routed to the output link of cell \( i_1 \) consecutively. Since packet \( p' \) is stored in cell \( i_1 \) at time \( t_0 - 1 \) and is stored in cell \( i_2 \) at time \( t - 1 \), and \( i_1 < i_2 \), it is clear that packet \( p' \) must be routed to the output link of cell \( i_1 \) at or before time \( t - 1 \). As such, it follows that packet \( p' \) and packet \( p' + 1 \) are routed to the output link of cell \( i_1 \) consecutively at or before time \( t \).

Assume as the induction hypothesis that packet \( p' \) and packet \( p' + 1 \) are routed to the output link of cell \( i \) consecutively at or before time \( t \), say at time \( t' - 1 \) and time \( t' \) with \( t' \leq t \), respectively, for some \( i_1 \leq i \leq i_2 - 2 \). As packet \( p' \) is routed to the output link of cell \( i \) at time \( t' - 1 \) and is stored in cell \( i_2 \) at time \( t - 1 \), and \( t' - 1 \leq t - 1 \), it must be the case that packet \( p' \) is routed into the fiber delay line in cell \( i' \) at time \( t' - 1 \) for some \( i + 1 \leq i' \leq i_2 \), and hence packet \( p' \) is stored in buffer \( b_{i'}(i' - 1) \) at time \( t' - 1 \) (see Figure 13(a)). Since \( i' \leq i_2 \leq k - 1 \) and we know from Lemma 5(ii) that packets stored in any one of the first \( k \) cells at any time are ordered according to their arrival times, we immediately see that packet \( p' \) is the latest arrival packet in cell \( i' \) at time \( t' - 1 \), and hence we have from (9) that

\[
W_{i'}(t') = 0. \tag{82}
\]

As packet \( p' \) is stored in cell \( i_1 \) at time \( t_0 - 1 \) and is stored in cell \( i' \) at time \( t' - 1 \), and \( i_1 \leq i < i' \), we must have \( t_0 - 1 < t' - 1 \), i.e., \( t_0 < t' \). Since packet \( p' + 1 \) is admitted into the network element at time \( t_0 \) and is routed to the output link of cell \( i \) at a later time \( t' \) (note that \( t_0 < t' \)), it must be the case that packet \( p' + 1 \) is stored in buffer \( b_{i'}(0) \) at time \( t' - 1 \) for some \( 0 \leq i'' \leq i \), switch \( i'' \) is set to the “cross” state at time \( t' \), and switch \( j \) is set to the “bar” state at time \( t' \) for \( j = i'' + 1, i'' + 2, \ldots, i \) (see Figure 13(b)).
Fig. 13. (a) Packet $p'$ at time $t' - 1$ in Case 1 in the proof of Lemma 6(iii); (b) Packet $p' + 1$ at time $t'$ in Case 1 in the proof of Lemma 6(iii).

Since packet $p'$ is stored in buffer $b_{i'}(\ell_{i'} - 1)$ at time $t' - 1$ and packet $p' + 1$ is stored in buffer $b_{i''}(0)$ at time $t' - 1$, it is clear that

$$q_{i'}(t' - 1) \neq 0 \text{ and } q_{i''}(t' - 1) \neq 0.$$  \hspace{1cm} (83)

Furthermore, as $0 \leq i'' < i < i' \leq i_2 \leq k - 1$ and we know from Lemma 5(ii) that packets stored in the first $k$ cells satisfy the ordered property in (A2) at all times, it then follows that

$$q_j(t' - 1) = 0, \text{ for } i'' + 1 \leq j \leq i' - 1.$$  \hspace{1cm} (84)

From (8), $0 \leq i'' < i' \leq k - 1$, and (83), we have

$$q^{(1)}(t' - 1) = \sum_{j=0}^{k-1} q_j(t' - 1) \neq 0.$$  \hspace{1cm} (85)

From (83) and (84), we can see that

$$j_{n-1}(t') = i'' \text{ and } j_n(t') = i', \text{ for some } 2 \leq n \leq n(t'),$$  \hspace{1cm} (86)

where $n(t')$ is the number of nonempty cells among the first $k$ cells at time $t' - 1$ and $j_{n-1}(t')$ and $j_n(t' - 1)$ are the indices of the $(n - 1)^{\text{th}}$ nonempty cell and the $n^{\text{th}}$ nonempty cell, respectively, among the first $k$ cells at time $t' - 1$ as defined in (C2). From (85), (86), (82), (16), and (17), we see that switch $i''$ and switch $i'$ are set to the “cross” state at time $t'$ and switch $j$ is set to the “bar” state at time $t'$ for $j = i'' + 1, i'' + 2, \ldots, i' - 1$.

As $i + 1 \leq i' \leq i_2$, we consider the two cases $i' = i + 1$ and $i + 1 < i' \leq i_2$ separately.

Subcase 1(a): $i' = i + 1$. Since packet $p'$ is stored in buffer $b_{i'}(\ell_{i'} - 1)$ at time $t' - 1$, packet $p' + 1$ is stored in buffer $b_{i''}(0)$ at time $t' - 1$, switch $i''$ and switch $i'$ are set to the “cross” state
at time $t'$, and switch $j$ is set to the “bar” state at time $t'$ for $j = i'' + 1, i'' + 2, \ldots, i' - 1$, it is easy to see that packet $p'$ is stored in buffer $b_{i'}(\ell_{i'} - 2)$ at time $t'$ and packet $p' + 1$ is stored in buffer $b_{i'}(\ell_{i'} - 1)$ at time $t'$ (see Figure 14), and it follows that packet $p'$ and packet $p' + 1$ are stored in buffer $b_{i'}(0)$ at time $t' + \ell_{i'} - 2$ and time $t' + \ell_{i'} - 1$, respectively. From (16), we see that switch $i'$ is set to the “cross” state at time $t' + \ell_{i'} - 1$ and time $t' + \ell_{i'}$, and hence packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i'$ consecutively at time $t' + \ell_{i'} - 1$ and time $t' + \ell_{i'}$, respectively. As packet $p'$ is routed to the output link of cell $i'$ at time $t' + \ell_{i'} - 1$ and is stored in cell $i_2$ at time $t - 1$, and in this case we have $i' = i + 1 \leq i_2 - 1$, we must have $t' + \ell_{i'} - 1 \leq t - 1$. Therefore, packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i' = i + 1$ consecutively at or before time $t$ in this case.

![Fig. 14. Packet $p'$ and packet $p' + 1$ at time $t'$ in Subcase 1(a) in the proof of Lemma 6(iii).](image)

Subcase 1(b): $i + 1 < i' \leq i_2$. As we know that packet $p'$ is routed to the output link of cell $i$ at time $t' - 1$ (from the induction hypothesis) and is stored in cell $i'$ at time $t' - 1$, we see from $i + 1 < i'$ in this case that packet $p'$ must be routed to the output link of cell $i + 1$ at time $t' - 1$. Since packet $p' + 1$ is stored in buffer $b_{i'}(0)$ at time $t' - 1$, switch $i''$ and switch $i'$ are set to the “cross” state at time $t'$, and switch $j$ is set to the “bar” state at time $t'$ for $j = i'' + 1, i'' + 2, \ldots, i' - 1$, it is clear from $i'' + 1 \leq i + 1 \leq i' - 1$ that packet $p' + 1$ is routed to the output link of cell $i + 1$ at time $t'$ (see Figure 15). Therefore, it follows from $t' \leq t$ that packet $p'$ and packet $p' + 1$ are also routed to the output link of cell $i + 1$ consecutively at or before time $t$ in this case.

![Fig. 15. Packet $p'$ and packet $p' + 1$ at time $t'$ in Subcase 1(b) in the proof of Lemma 6(iii).](image)

Case 2: Packet $p'$ is not stored in the first $k$ cells at time $t - 1$. In the following, we show by induction on $i$ that packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i$ consecutively at or before time $t$ for $i = i_1, i_1 + 1, \ldots, k - 1$. By the same argument as in Case 1 in the proof
of Lemma 6(iii), we can show that packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i_1$ consecutively at or before time $t$.

Assume as the induction hypothesis that packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i$ consecutively at or before time $t$, say at time $t' - 1$ and time $t'$ with $t' \leq t$, respectively, for some $i_1 \leq i \leq k - 2$. As packet $p'$ is routed to the output link of cell $i$ at time $t' - 1$ and is not stored in the first $k$ cells at time $t - 1$, and $t' - 1 \leq t - 1$, it must be the case that either packet $p'$ is routed into the fiber delay line in cell $i'$ at time $t' - 1$ for some $i' + 1 \leq i' \leq k - 1$ (see Figure 16(a)), or packet $p'$ is routed to the output link of cell $k - 1$ at time $t' - 1$ (see Figure 16(b)).

![Diagram of packet routing](image)

**Fig. 16.** Packet $p'$ at time $t' - 1$ in Case 2 in the proof of Lemma 6(iii).

If packet $p'$ is routed into the fiber delay line in cell $i'$ at time $t' - 1$ for some $i' + 1 \leq i' \leq k - 1$, then it is clear that packet $p'$ is stored in buffer $b_{i'}(\ell_{i'} - 1)$ at time $t' - 1$. Furthermore, by using the same argument as in Case 1 in the proof of Lemma 6(iii) above, we can show that packet $p' + 1$ is stored in buffer $b_{i'}(0)$ at time $t' - 1$ for some $0 \leq i'' \leq i$, switch $i''$ and switch $i'$ are set to the “cross” state at time $t'$ and switch $j$ is set to the “bar” state at time $t'$ for $j = i'' + 1, i'' + 2, \ldots, i' - 1$.

As $i + 1 \leq i' \leq k - 1$, we consider the two cases $i' = i + 1$ and $i + 1 < i' \leq k - 1$ separately.

**Subcase 2(a):** $i' = i + 1$. By using the same argument as in Subcase 1(a) in the proof of Lemma 6(iii) above, we can show that packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i'$ consecutively at time $t' + \ell_{i'} - 1$ and time $t' + \ell_{i'}$, respectively. As packet $p'$ is routed to the output link of cell $i'$ at time $t' + \ell_{i'} - 1$ and is not stored in the first $k$ cells at time $t - 1$, it follows from $i' \leq k - 1$ that we must have $t' + \ell_{i'} - 1 \leq t - 1$. Therefore, packet $p'$ and packet $p' + 1$ are routed to the output link of cell $i' = i + 1$ consecutively at or before time $t$ in this case.
Subcase 2(b): \( i + 1 < i' \leq k - 1 \). By using the same argument as in Subcase 1(b) in the proof of Lemma 6(iii) above, we can show that packet \( p' \) and packet \( p' + 1 \) are also routed to the output link of cell \( i + 1 \) consecutively at or before time \( t \) in this case.

On the other hand, if packet \( p' \) is routed to the output link of cell \( k - 1 \) at time \( t' - 1 \), then we must have \( t_0 - 1 < t' - 1 \) (as packet \( p' \) is stored in cell \( i_1 \) at time \( t_0 - 1 \) and \( i_1 \leq k - 1 \)), i.e., \( t_0 < t' \). Since packet \( p' + 1 \) is admitted into the network element at time \( t_0 \) and we know from the induction hypothesis that packet \( p' + 1 \) is routed to the output link of cell \( i \) at a later time \( t' \), it must be the case that packet \( p' + 1 \) is stored in buffer \( b_{i'}(0) \) at time \( t' - 1 \) for some \( 0 \leq i'' \leq i \) and switch \( i'' \) is set to the “cross” state at time \( t' \) and switch \( j \) is set to the “bar” state at time \( t' \) for \( j = i'' + 1, i'' + 2, \ldots, i \). Thus, we have

\[
q_{i''}(t' - 1) \neq 0. \tag{87}
\]

It follows from (8), \( 0 \leq i'' \leq i \leq k - 2 \), and (87) that

\[
q(1)(t' - 1) = \sum_{j=0}^{k-1} q_j(t' - 1) \neq 0. \tag{88}
\]

As packet \( p' \) is stored in cell \( i_1 \) at time \( t_0 - 1 \) and is routed to the output link of cell \( k - 1 \) at time \( t' - 1 \) and \( t_0 - 1 < t' - 1 \), we see from Lemma 5(iii) that packet \( p' \) is the earliest arrival packet in the first \( k \) cells at time \( t' - 2 \). Since packet \( p' \) is routed to the output link of cell \( k - 1 \) at time \( t' - 1 \) so that it is not stored in the first \( k \) cells at time \( t' - 1 \), packet \( p' + 1 \) is stored in buffer \( b_{i'}(0) \) at time \( t' - 1 \), and \( 0 \leq i'' \leq i \leq k - 2 \), it follows that packet \( p' + 1 \) is the “earliest” arrival packet in the first \( k \) cells at time \( t' - 1 \). Since we also know from Lemma 5(ii) that packets stored in the first \( k \) cells satisfy the ordered property in (A2) at all times, we have

\[
q_j(t' - 1) = 0, \text{ for } i'' + 1 \leq j \leq k - 1. \tag{89}
\]

From (87) and (89), we can see that

\[
j_{n(t')}(t') = i'', \tag{90}
\]

where \( n(t') \) is the number of nonempty cells among the first \( k \) cells at time \( t' - 1 \) and \( j_{n(t')}(t') \) is the largest index of a nonempty cell among the first \( k \) cells at time \( t' - 1 \) as defined in (C2).

As packet \( p' \) is routed to the output link of cell \( k - 1 \) at time \( t' - 1 \), we have

\[
d_{k-1}(t' - 1) = 1, \tag{91}
\]

From (88), (90), (91), (16), and (18), we see that switch \( i'' \) is set to the “cross” state at time \( t' \) and switch \( j \) is set to the “bar” state at time \( t' \) for \( j = i'' + 1, i'' + 2, \ldots, k - 1 \). Since packet \( p' + 1 \) is stored in buffer \( b_{i'}(0) \) at time \( t' - 1 \) and \( i'' + 1 \leq i + 1 \leq k - 1 \), it then follows that packet \( p' + 1 \) is routed to the output link of cell \( i + 1 \) at time \( t' \) (see Figure 17). Therefore, it follows from \( t' \leq t \) that packet \( p' \) and packet \( p' + 1 \) are routed to the output link of cell \( i + 1 \) consecutively at or before time \( t \). The induction is completed.
Lemma 7 Suppose that (A1) is satisfied and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3).

(i) Suppose that packet $p$ is stored in buffer $b_{i_1}(j_1)$ at time $t_1$ and is stored in cell $i_2$ at time $t_2$ for some $k \leq i_1 \leq i_2 \leq 2k$, $0 \leq j \leq \ell_{i_1 - 1}$, and $t_1 \leq t_2$. Then packet $p$ is stored in buffer $b_{i_2}((j_1 + t_1 - t_2) \mod \ell_{i_2})$ at time $t_2$.

(ii) Suppose that packet $p$ is routed to the output link of cell $k-1$ at time $t_1$ and is stored in cell $i_2$ at time $t_2$ for some $k \leq i_2 \leq 2k$. Then packet $p$ is stored in buffer $b_{i_2}((t_1 - t_2 - 1) \mod \ell_{i_2})$ at time $t_2$.

Proof. (i) Suppose that packet $p$ is stored in buffer $b_{i_2}(j_2)$ at time $t_2$. Let $n_i$ be the number of times that packet $p$ is routed into the fiber delay line in cell $i$ during the time period $[t_1 + 1, t_2]$ for $i = i_1, i_1 + 1, \ldots, i_2$. As packet $p$ is stored in buffer $b_{i_1}(j_1)$ at time $t_1$, we see that packet $p$ is stored in buffer $b_{i_1}(0)$ at time $t_1 + j_1 + n_{i_1} \cdot \ell_{i_1}$, is stored in buffer $b_{i_{1+1}}(0)$ at time $t_1 + j_1 + n_{i_1} \cdot \ell_{i_1} + n_{i_{1+1}} \cdot \ell_{i_{1+1}}$ (in the case that $n_{i_{1+1}} \geq 1$), $\ldots$, is stored in buffer $b_{i_{i_2-1}}(0)$ at time $t_1 + j_1 + n_{i_1} \cdot \ell_{i_1} + n_{i_{1+1}} \cdot \ell_{i_{1+1}} + \cdots + n_{i_{i_2-1}} \cdot \ell_{i_{i_2-1}}$ (in the case that $n_{i_{i_2-1}} \geq 1$), and is stored in buffer $b_{i_2}(j_2)$ at time $t_1 + j_1 + n_{i_1} \cdot \ell_{i_1} + n_{i_{1+1}} \cdot \ell_{i_{1+1}} + \cdots + n_{i_{i_2-1}} \cdot \ell_{i_{i_2-1}} + (n_{i_{i_2-1}} - 1) \cdot \ell_{i_{i_2-1}} + j_2$. Thus, we have

$$t_2 = t_1 + j_1 + \sum_{i=i_1}^{i_2} n_i \cdot \ell_i - j_2.$$ (92)

From $k \leq i_1 \leq i_2 \leq 2k$ and (4), we have

$$\ell_i \mod \ell_{i_2} = 0, \text{ for } i_1 \leq i \leq i_2.$$ (93)

It then follows from $0 \leq j_2 \leq \ell_{i_2} - 1$, (92), and (93) that

$$j_2 = j_2 \mod \ell_{i_2}$$

$$= (j_1 + t_1 - t_2 + \sum_{i=i_1}^{i_2} n_i \cdot \ell_i) \mod \ell_{i_2}$$

$$= (j_1 + t_1 - t_2) \mod \ell_{i_2}.$$
(ii) As packet \( p \) is routed to the output link of cell \( k - 1 \) at time \( t_1 \) and is stored in cell \( i_2 \) at time \( t_2 \) for some \( k \leq i_2 < 2k \), it is clear that \( t_1 \leq t_2 \) and packet \( p \) is stored in buffer \( b_{i_2}(\ell_{i_2} - 1) \) at time \( t_1 \) for some \( k \leq i_1 \leq i_2 \). Therefore, we have from Lemma 7(ii) that packet \( p \) is stored in buffer \( b_{i_2}(\ell_{i_2} - 1 + t_1 - t_2) \mod \ell_{i_2} = b_{i_2}((t_1 - t_2 - 1) \mod \ell_{i_2}) \) at time \( t_2 \).

Lemma 8 Suppose that \( \ell_{b_0}^{k-1} \in \mathcal{A}_k \) \((A1)\) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in \((C1)-(C3)\). Also suppose that the ordered property in \((A2)\) and the FIFO departure property in \((P4)\) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied up to time \( t - 1 \). Assume that cell \( i_2 \) is nonempty at time \( t - 1 \) for some \( 0 \leq i_2 \leq 2k \), say packet \( p \) is stored in cell \( i_2 \) at time \( t - 1 \). If packet \( p + 1 \) is routed to the input link of cell \( i_2 \) at time \( t \), then packet \( p \) is stored in buffer \( b_{i_2}(\ell_{i_2} - 1) \) at time \( t - 1 \).

Proof. Suppose that packet \( p + 1 \) is routed to the input link of cell \( i_2 \) at time \( t \). Assume that packet \( p + 1 \) is admitted into the network element at time \( t_0 \). It is clear that \( t_0 \leq t \) and packet \( p \) has been admitted into the network element before time \( t_0 \). As packet \( p \) is stored in cell \( i_2 \) at time \( t - 1 \) and \( t_0 - 1 \leq t - 1 \), we then see that packet \( p \) is stored in cell \( i_1 \) at time \( t_0 - 1 \) for some \( 0 \leq i_1 \leq i_2 \). Since packet \( p + 1 \) has not arrived at the network element yet at time \( t_0 - 1 \), it then follows that packet \( p \) is the latest arrival packet in the \( 2k + 1 \) cells at time \( t_0 - 1 \). In particular, packet \( p \) is the latest arrival packet in cell \( i_1 \) at time \( t_0 - 1 \).

As packet \( p + 1 \) is routed to the input link of cell \( i_2 \) at time \( t \), we see that packet \( p + 1 \) is either stored in buffer \( b_{i_3}(0) \) at time \( t - 1 \) for some \( 0 \leq i_3 < i_2 \) or admitted into the network element at time \( t \). We then consider the following four possible cases. Note that the assumptions in the statement of Lemma 6 hold as we assume that the ordered property in \((A2)\) and the FIFO departure property in \((P4)\) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied up to time \( t - 1 \).

Case 1: Packet \( p + 1 \) is stored in buffer \( b_{i_3}(0) \) at time \( t - 1 \), where \( k \leq i_3 < i_2 \leq 2k \). Since \( 0 \leq i_1 \leq i_2 \), we consider the two subcases \( 0 \leq i_1 \leq k - 1 \) and \( k \leq i_1 \leq i_2 \) separately.

Subcase 1(a): \( 0 \leq i_1 \leq k - 1 \). In this subcase, packet \( p \) is stored in the first \( k \) cells at time \( t_0 - 1 \) and is stored in the last \( k + 1 \) cells at time \( t - 1 \). It follows from Lemma 6(iii) that packet \( p \) and packet \( p + 1 \) are routed to the output link of cell \( k - 1 \) consecutively at or before time \( t \), say at time \( t' - 1 \) and time \( t' \) with \( t' \leq t \), respectively. As packet \( p \) is routed to the output link of cell \( k - 1 \) at time \( t' - 1 \) and is stored in cell \( i_2 \) at time \( t - 1 \), and \( k < i_2 \leq 2k \), we see from Lemma 7(ii) that packet \( p \) is stored in buffer \( b_{i_2}((t' - t - 1) \mod \ell_{i_2}) \) at time \( t - 1 \). Since packet \( p + 1 \) is routed to the output link of cell \( k - 1 \) at time \( t' \) and is stored in buffer \( b_{i_3}(0) \) at time \( t - 1 \), and \( k \leq i_3 < 2k \), we see from Lemma 7(ii) that

\[
0 = (t' - (t - 1) - 1) \mod \ell_{i_3} = (t' - t) \mod \ell_{i_3},
\]  

(94)
Note that in this subcase we have from $k \leq i_3 < i_2 \leq 2k$ and (4) that $(\ell_{i_3} \mod \ell_{i_2}) = 0$. It then follows from $(\ell_{i_3} \mod \ell_{i_2}) = 0$ and (94) that
\[
(t' - t - 1) \mod \ell_{i_2} = [(t' - t - 1) \mod \ell_{i_2}] \mod \ell_{i_2} = (\ell_{i_2} - 1) \mod \ell_{i_2} = \ell_{i_2} - 1.
\] (95)

Therefore, we see from (95) that packet $p$ is stored in buffer $b_{i_2}((\ell_{i_2} - 1)$ at time $t - 1$ in this subcase.

Subcase 1(b): $k \leq i_1 \leq i_2$. In this subcase, packet $p$ is stored in the last $k + 1$ cells at time $t_0 - 1$. It follows from Lemma 6(ii) that packet $p + 1$ is routed to the output link of cell $k - 1$ at time $t_0 + w_i_1(t_0)$. As packet $p + 1$ is stored in buffer $b_{i_2}(0)$ at time $t - 1$ in this case and $k \leq i_3 \leq 2k$, we then see from Lemma 7(ii) that
\[
(t_0 + w_i_1(t_0) - t) \mod \ell_{i_3} = 0.
\] (96)

Note we have shown that packet $p$ is the latest arrival packet in cell $i_1$ at time $t_0-1$. Since in this subcase we also have $k \leq i_1 \leq i_2 \leq 2k$, it follows from (4) that $(\ell_{i_1} \mod \ell_{i_2}) = 0$. If $w_i_1(t_0) = 0$, then we have from (10) that packet $p$ is stored in buffer $b_{i_1}((\ell_{i_1} - 1)$ at time $t_0 - 1$. As packet $p$ is stored in cell $i_2$ at time $t - 1$, $k \leq i_1 \leq i_2 \leq 2k$, and $t_0 - 1 \leq t - 1$, we see from Lemma 7(i) and $(\ell_{i_1} \mod \ell_{i_2}) = 0$ that packet $p$ is stored in buffer $b_{i_2}(((\ell_{i_1} - 1) + (t_0 - 1) - (t - 1)) \mod \ell_{i_2}) = b_{i_2}((t_0 - t - 1) \mod \ell_{i_2})$ at time $t - 1$. On the other hand, if $w_i_1(t_0) \neq 0$, then we have from (10) that packet $p$ is stored in buffer $b_{i_1}(w_i_1(t_0) - 1)$ at time $t_0 - 1$, and we also see from Lemma 7(i) that packet $p$ is stored in buffer $b_{i_2}(((w_i_1(t_0) - 1) + (t_0 - 1) - (t - 1)) \mod \ell_{i_2}) = b_{i_2}((t_0 + w_i_1(t_0) - t - 1) \mod \ell_{i_2})$ at time $t - 1$. As such, packet $p$ is stored in buffer $b_{i_2}((t_0 + w_i_1(t_0) - t - 1) \mod \ell_{i_2})$ at time $t - 1$ no matter $w_i_1(t_0) = 0$ or $w_i_1(t_0) \neq 0$. From $(\ell_{i_3} \mod \ell_{i_2}) = 0$ and (96), we have
\[
(t_0 + w_i_1(t_0) - t - 1) \mod \ell_{i_2} = [(t_0 + w_i_1(t_0) - t - 1) \mod \ell_{i_3}] \mod \ell_{i_2} = (\ell_{i_3} - 1) \mod \ell_{i_2} = \ell_{i_2} - 1.
\] (97)

Therefore, we see from (97) that packet $p$ is stored in buffer $b_{i_2}((\ell_{i_2} - 1)$ at time $t - 1$ in this subcase.

Case 2: Packet $p + 1$ is stored in buffer $b_{i_3}(0)$ at time $t - 1$, where $0 \leq i_3 \leq k - 1$ and $k \leq i_2 \leq 2k$. As packet $p + 1$ is stored in buffer $b_{i_3}(0)$ at time $t - 1$ and is routed to the input link of cell $i_2$ at time $t$, and $i_3 \leq k - 1 < i_2$, it is easy to see that packet $p + 1$ is routed to the output link of cell $k - 1$ at time $t$. Since $0 \leq i_1 \leq i_2$, we consider the two subcases $0 \leq i_1 \leq k - 1$ and $k \leq i_1 \leq i_2$ separately.

Subcase 2(a): $0 \leq i_1 \leq k - 1$. In this subcase, packet $p$ is stored in the first $k$ cells at time $t_0 - 1$ and is stored in the last $k + 1$ cells at time $t - 1$. It follows from Lemma 6(iii) that packet $p$ and packet $p + 1$ are routed to the output link of cell $k - 1$ consecutively at or before time
Since packet $p$ is stored in cell $i_2$ at time $t = t_1$ and $k \leq i_2 \leq 2k$, it must be the case that switch $i$ is set to the “bar” state at time $t - 1$ for $i = k, k + 1, \ldots, i_2 - 1$ and switch $i_2$ is set to the “cross” state at time $t - 1$ so that packet $p$ is stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t - 1$ in this subcase.

**Subcase 2(b):** $k \leq i_1 \leq i_2$. In this subcase, packet $p$ is stored in the last $k + 1$ cells at time $t_0 - 1$. It follows from Lemma 6(ii) that packet $p + 1$ is routed to the output link of cell $k - 1$ at time $t_0 + w_{i_1}(t_0)$. As in this case we have shown that packet $p + 1$ is routed to the output link of cell $k - 1$ at time $t$, we then see that

$$t = t_0 + w_{i_1}(t_0).$$

If $w_{i_1}(t_0) = 0$, then we have from (98) that $t = t_0$, namely, packet $p + 1$ is admitted into the network element at time $t$, and this contradicts to the assumption that packet $p + 1$ is stored in buffer $b_{i_3}(0)$ at time $t - 1$ in this case. Therefore, we must have $w_{i_1}(t_0) \neq 0$. As we have shown that packet $p$ is the latest arrival packet in cell $i_1$ at time $t_0 - 1$, we see from (10) that packet $p$ is stored in buffer $b_{i_1}(w_{i_1}(t_0) - 1)$ at time $t_0 - 1$. Thus, we have from (98) that packet $p$ is stored in buffer $b_{i_1}(0)$ at time $t_0 + w_{i_1}(t_0) - 2 = t - 2$. Since packet $p$ is stored in cell $i_2$ at time $t - 1$ and in this subcase we have $k \leq i_1 \leq i_2$, we can see that either $i_1 = i_2$ and switch $i_2$ is set to the “bar” state at time $t - 1$ so that packet $p$ is stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t - 1$, or $i_1 < i_2$, switch $i_1$ and switch $i_2$ are set to the “cross” state at time $t - 1$, and switch $i$ is set to the “bar” state at time $t - 1$ for $i = i_1 + 1, i_1 + 2, \ldots, i_2 - 1$ so that packet $p$ is also stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t - 1$.

**Case 3:** Packet $p + 1$ is stored in buffer $b_{i_3}(0)$ at time $t - 1$, where $0 \leq i_3 < i_2 \leq k - 1$. Since $0 \leq i_1 \leq i_2$, we consider the two subcases $i_1 = i_2$ and $i_1 < i_2$ separately.

**Subcase 3(a):** $i_1 = i_2$. We show by contradiction that this subcase cannot happen. In this subcase, we have from $i_1 = i_2$ and $0 < i_2 \leq k - 1$ that $0 < i_1 \leq k - 1$, i.e., packet $p$ is stored in the first $k$ cells at time $t_0 - 1$. It follows from Lemma 6(i) that packet $p + 1$ is routed to the input link of cell $i_1$ at time $t_0 + w_{i_1}(t_0)$. As we assume that packet $p + 1$ is routed to the input link of cell $i_2$ at time $t$ and in this subcase we have $i_1 = i_2$, we then see that $t = t_0 + w_{i_1}(t_0)$. If $w_{i_1}(t_0) = 0$, then we have $t = t_0$, namely, packet $p + 1$ is admitted into the network element at time $t$, and this contradicts to the assumption that packet $p + 1$ is stored in buffer $b_{i_3}(0)$ at time $t - 1$ in this case. On the other hand, if $w_{i_1}(t_0) \neq 0$, then we see from (10) that packet $p$ is stored in buffer $b_{i_1}(w_{i_1}(t_0) - 1)$ at time $t_0 - 1$ since we have shown that packet $p$ is the latest arrival packet in cell $i_1$ at time $t_0 - 1$. Thus, it is clear that packet $p$ is stored in buffer $b_{i_1}(0)$ at time $t_0 + w_{i_1}(t_0) - 2$. From $0 < i_1 \leq k - 1$ and (16), we see that switch $i_1$ is set to the “cross” state at time $t_0 + w_{i_1}(t_0) - 1$, and hence packet $p$ is routed to the output link of cell $i_1$ at time $t_0 + w_{i_1}(t_0) - 1 = t - 1$, contradicting to the assumption that packet $p$ is stored in cell $i_2 = i_1$ at time $t - 1$. 


Subcase 3(b): \( i_1 < i_2 \). In this subcase, we have \( 0 \leq i_1 < i_2 \leq k - 1 \), i.e., packet \( p \) is stored in the first \( k \) cells at time \( t_0 - 1 \) and time \( t - 1 \). It follows from Lemma 6(iii) that packet \( p \) and packet \( p+1 \) are routed to the output link of cell \( i_2 - 1 \), i.e., the input link of cell \( i_2 \), consecutively at or before time \( t \). As we assume that packet \( p+1 \) is routed to the input link of cell \( i_2 \) at time \( t \), we then see that packet \( p \) must be routed to the input link of cell \( i_2 \) at time \( t - 1 \). Since we also assume that packet \( p \) is stored in cell \( i_2 \) at time \( t - 1 \), it must be the case that switch \( i_2 \) is set to the “cross” state at time \( t - 1 \) and hence packet \( p \) is stored in buffer \( b_{i_2}(\ell_{i_2} - 1) \) at time \( t - 1 \) in this subcase.

Case 4: Packet \( p + 1 \) is admitted into the network element at time \( t \). In this case, we have \( t_0 = t \) and we immediately see that \( i_1 = i_2 \). We consider the two subcases \( 0 \leq i_1 \leq k - 1 \) and \( k \leq i_1 \leq 2k \) separately.

Subcase 4(a): \( 0 \leq i_1 \leq k - 1 \). In this subcase, packet \( p \) is stored in the first \( k \) cells at time \( t_0 - 1 \). It follows from Lemma 6(i) and \( t_0 = t \) that packet \( p + 1 \) is routed to the input link of cell \( i_1 \) at time \( t_0 + w_{i_1}(t_0) = t + w_{i_1}(t) \). As we assume that packet \( p + 1 \) is routed to the input link of cell \( i_2 \) at time \( t \) and in this case we have \( i_1 = i_2 \), we then see that \( t + w_{i_1}(t) = t \), i.e., \( w_{i_1}(t) = 0 \). Since packet \( p \) is the latest arrival packet in cell \( i_1 \) at time \( t_0 - 1 = t - 1 \), we have from (10) that packet \( p \) is stored in buffer \( b_{i_1}(\ell_{i_1} - 1) \) at time \( t - 1 \). Therefore, we see from \( i_1 = i_2 \) that packet \( p \) is stored in buffer \( b_{i_2}(\ell_{i_2} - 1) \) at time \( t - 1 \) in this subcase.

Subcase 4(b): \( k \leq i_1 \leq 2k \). In this subcase, packet \( p \) is stored in the last \( k + 1 \) cells at time \( t_0 - 1 \). It follows from Lemma 6(ii) and \( t_0 = t \) that packet \( p + 1 \) is routed to the output link of cell \( k - 1 \) at time \( t_0 + w_{i_1}(t_0) = t + w_{i_1}(t) \). As packet \( p + 1 \) is admitted into the network element at time \( t \) and is routed to the input link of cell \( i_2 \) at time \( t \), \( i_2 = i_1 \), and \( k \leq i_1 \leq 2k \), we then see that packet \( p + 1 \) is also routed to the output link of cell \( k - 1 \) at time \( t \). Thus, we have \( t + w_{i_1}(t) = t \), i.e., \( w_{i_1}(t) = 0 \). Therefore, by using the same argument as in Subcase 4(a) in the proof of Lemma 8 above, we can also show that packet \( p \) is stored in buffer \( b_{i_2}(\ell_{i_2} - 1) \) at time \( t - 1 \) in this subcase.

Lemma 9 Suppose that the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the circularly contiguous property in (A3) is satisfied at time \( t - 1 \). Then packets stored in any one of the \( 2k + 1 \) cells at time \( t - 1 \) depart from the output link of that cell in the FIFO order at time \( t \).

Proof. We prove Lemma 9 by contradiction. Suppose that a packet, say packet \( p \), is routed from the fiber delay line in cell \( i \) to the output link of cell \( i \) at time \( t \) for some \( 0 \leq i \leq 2k \), and it is not the earliest arrival packet in cell \( i \) at time \( t - 1 \). It is clear that packet \( p \) is stored in buffer \( b_i(0) \) at time \( t - 1 \) and switch \( i \) is set to the “cross” state at time \( t \). Furthermore, as we have from Lemma 5(ii) that packets stored in any one of the first \( k \) cells at time \( t - 1 \) depart from the output link of that cell in the FIFO order at time \( t \), it must be the case that \( k \leq i \leq 2k \).
As packet \( p \) is not the earliest arrival packet in cell \( i \) at time \( t - 1 \), we see from the definition of \( r_i(t) \) that \( r_i(t) \neq 0 \). Since \( k \leq i \leq 2k \), \( q_i(t - 1) \neq 0 \) (note that packet \( p \) is stored in buffer \( b_i(0) \) at time \( t - 1 \)), \( r_i(t) \neq 0 \), and switch \( i \) is set to the “cross” state at time \( t \), we then see from (20) that \( r_i(t) + q_i(t - 1) \leq \ell_i \). As such, it follows from \( r_i(t) \neq 0 \), \( r_i(t) + q_i(t - 1) \leq \ell_i \), and Lemma 2(i) (note that we assume that the circularly contiguous property in (A3) is satisfied at time \( t - 1 \)) that buffer \( b_i(0) \) is empty at time \( t - 1 \), and we have reached a contradiction. ■

**Lemma 10** Suppose that the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the ordered property in (A2) is satisfied at time \( t - 1 \) and time \( t \) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied up to time \( t \). Assume that cell \( i \) is nonempty at time \( t - 1 \) for some \( 0 \leq i \leq 2k \) and the “latest” arrival packet in cell \( i \) at time \( t - 1 \) is packet \( p' \). If there is a packet routed to the input link of cell \( i \) at time \( t \), then that packet is packet \( p' + 1 \).

**Proof.** We prove Lemma 10 by contradiction. Suppose that there is a packet, say packet \( p_1 \), routed to the input link of cell \( i \) at time \( t \) and \( p_1 \neq p' + 1 \). Then there are only two possible cases to consider.

**Case 1:** Packet \( p_1 \) is stored in buffer \( b_{i_1}(0) \) for some \( 0 \leq i_1 < i \) at time \( t - 1 \), switch \( i_1 \) is set to the “cross” state at time \( t \), and switch \( j \) is set to the “bar” state at time \( t \) for \( j = i_1 + 1, i_1 + 2, \ldots, i - 1 \). In this case, we have \( p_1 > p' \) as packet \( p_1 \) is stored in cell \( i_1 \) at time \( t - 1 \), packet \( p' \) is stored in cell \( i \) at time \( t - 1 \), \( i_1 < i \), and the ordered property in (A2) is satisfied at time \( t - 1 \). It follows from \( p_1 > p' \) and \( p_1 \neq p' + 1 \) that \( p_1 > p' + 1 \). As packet \( p_1 \) is stored in cell \( i_1 \) at time \( t - 1 \), it must be admitted into the network element at or before time \( t - 1 \), and it follows from \( p_1 > p' + 1 \) that packet \( p' + 1 \) must be admitted into the network element before time \( t - 1 \). As we assume that the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied up to time \( t \), packet \( p' \) is stored in cell \( i \) at time \( t - 1 \), and \( p' + 1 > p' \), it is easy to see that packet \( p' + 1 \) is stored in the \( 2k + 1 \) cells at time \( t - 1 \), say packet \( p' + 1 \) is stored in cell \( i_2 \) at time \( t - 1 \). Since the ordered property in (A2) is satisfied at time \( t - 1 \), \( p_1 > p' + 1 > p' \), and packet \( p' \) is the latest arrival packet in cell \( i \) at time \( t - 1 \), we then see that \( i_1 \leq i_2 < i \).

If \( i_1 = i_2 \), then it is clear that packet \( p' + 1 \) is stored in buffer \( b_{i_2}(j_2) \) at time \( t - 1 \) for some \( 1 \leq j_2 \leq \ell_{i_2} - 1 \) since packet \( p_1 \) is stored in buffer \( b_{i_1}(0) = b_{i_2}(0) \) at time \( t - 1 \). Thus, packet \( p' + 1 \) is stored in buffer \( b_{i_2}(j_2 - 1) \) at time \( t \). On the other hand, if \( i_1 < i_2 \), then we see from \( i_1 + 1 \leq i_2 \leq i - 1 \) that switch \( i_2 \) is set to the “bar” state at time \( t \) in this case, and hence packet \( p' + 1 \) is still stored in cell \( i_2 \) at time \( t \). As such, packet \( p' + 1 \) is stored in cell \( i_2 \) at time \( t \) no matter \( i_1 = i_2 \) or \( i_1 < i_2 \).

Furthermore, as packet \( p_1 \) is routed to the input link of cell \( i \) at time \( t \), it is easy to see that packet \( p_1 \) is either stored in buffer \( b_{i_3}(\ell_{i_3} - 1) \) at time \( t \) for some \( i \leq i_3 \leq 2k \) or routed to the
departure link of the network element at time $t$. If packet $p_1$ is stored in buffer $b_{i_3}(l_{i_3} - 1)$ at time $t$ for some $i \leq i_3 \leq 2k$, then from the fact that packet $p' + 1$ is stored in cell $i_2$ at time $t$, $p_1 > p' + 1$, and $i_3 \geq i > i_2$, we can see that the ordered property in (A2) is not satisfied at time $t$, and we have reached a contradiction. On the other hand, if packet $p_1$ is routed to the departure link of the network element at time $t$, then from the fact that packet $p' + 1$ is stored in cell $i_2$ at time $t$ and $p_1 > p' + 1$, we can see that the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is not satisfied at time $t$, and we have also reached a contradiction.

Case 2: Packet $p_1$ is admitted into the network element at time $t$ and switch $j$ is set to the “bar” state at time $t$ for $j = 0, 1, \ldots, i - 1$. In this case, we also have $p_1 > p'$ as packet $p_1$ arrives at the network element later than packet $p'$. It follows from $p_1 > p'$ and $p_1 \neq p' + 1$ that $p_1 > p' + 1$. As packet $p_1$ is admitted into the network element at time $t$ in this case, it follows from $p_1 > p' + 1$ that packet $p' + 1$ must be admitted into the network element before time $t$. As we assume that the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied up to time $t$, packet $p'$ is stored in cell $i$ at time $t - 1$, and $p' + 1 > p'$, it is easy to see that packet $p' + 1$ is stored in the $2k + 1$ cells at time $t - 1$, say packet $p' + 1$ is stored in cell $i_2$ at time $t - 1$. Since the ordered property in (A2) is satisfied at time $t - 1$, $p' + 1 > p'$, and packet $p'$ is the latest arrival packet in cell $i$ at time $t - 1$, we then see that $0 \leq i_2 < i$.

From $0 \leq i_2 \leq i - 1$, we can see that switch $i_2$ is set to the “bar” state at time $t$ in this case, and hence packet $p' + 1$ is still stored in cell $i_2$ at time $t$. By using the same argument as in the last paragraph in Case 1 in the proof of Lemma 10 above, we can also reach a contradiction and the proof is completed.

Lemma 11 Suppose that the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied up to time $t - 1$. Then we have $q(t') \leq \sum_{j=k}^{2k} \ell_j$ for $t' = 0, 1, \ldots, t - 1$ and the maximum buffer usage property in (P3) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at time $t$.

Proof. Note that as we have shown in Lemma 4 that the flow conservation property in (P1) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times, we see that (5) holds at all times, i.e.,

$$q(t') = q(t' - 1) + a(t') - d(t') - \ell(t'),$$

for $t' \geq 1$. (99)

We first show by induction on $t'$ that $q(t') \leq \sum_{j=k}^{2k} \ell_j$ for $t' = 0, 1, \ldots, t - 1$. As the network element in Figure 1 is started from an empty system at time 0, we have $q(0) = 0 \leq \sum_{j=k}^{2k} \ell_j$. Assume as the induction hypothesis that $q(t') \leq \sum_{j=k}^{2k} \ell_j$ for some $0 \leq t' \leq t - 2$. If $q(t') \leq$
\[ \sum_{j=k}^{2k} \ell_j - 1, \text{ then it is clear from (99) and } a(t' + 1), d(t' + 1), \text{ and } \ell(t' + 1) \text{ can only be 0 or 1 that} \]
\[ q(t' + 1) = q(t') + a(t' + 1) - d(t' + 1) - \ell(t' + 1) \leq \left( \sum_{j=k}^{2k} \ell_j - 1 \right) + 1 - 0 - \sum_{j=k}^{2k} \ell_j (100) \]

On the other hand, if \( q(t') = \sum_{j=k}^{2k} \ell_j \), then we consider the two cases \( c(t' + 1) = 0 \) and \( c(t' + 1) = 1 \) separately.

**Case 1:** \( c(t' + 1) = 0 \). In this case, we have from \( q(t') - c(t' + 1) = \sum_{j=k}^{2k} \ell_j \) and (13) that \( \ell(t' + 1) = a(t' + 1) \). As we assume that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied at time \( t' + 1 \) (note that \( t' + 1 \leq t - 1 \)), we have from (6) and \( c(t' + 1) = 0 \) that \( d(t' + 1) = 0 \). As such, it follows from (99), \( q(t') = \sum_{j=k}^{2k} \ell_j \), \( d(t' + 1) = 0 \), and \( \ell(t' + 1) = a(t' + 1) \) that
\[ q(t' + 1) = q(t') + a(t' + 1) - d(t' + 1) - \ell(t' + 1) = \sum_{j=k}^{2k} \ell_j. \]  
(101)

**Case 2:** \( c(t' + 1) = 1 \). In this case, we have from (6), \( c(t' + 1) = 1 \), and \( q(t') + a(t' + 1) \geq \sum_{j=k}^{2k} \ell_j > 0 \) that \( d(t' + 1) = 1 \). As such, it follows from (99), \( q(t') = \sum_{j=k}^{2k} \ell_j, a(t' + 1) \) and \( \ell(t' + 1) \) can only be 0 or 1, and \( d(t' + 1) = 1 \) that
\[ q(t' + 1) = q(t') + a(t' + 1) - d(t' + 1) - \ell(t' + 1) \leq \sum_{j=k}^{2k} \ell_j + 1 - 1 - 0 = \sum_{j=k}^{2k} \ell_j. \]  
(102)

Therefore, we have from (100)–(102) that \( q(t' + 1) \leq \sum_{j=k}^{2k} \ell_j \), and the induction is completed.

Now we show that the maximum buffer usage property in (P3) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied at time \( t \). As we have shown that \( q(t - 1) \leq \sum_{j=k}^{2k} \ell_j \) and \( c(t) \) can only be 0 or 1, it is clear that \( q(t - 1) - c(t) \leq \sum_{j=k}^{2k} \ell_j \) and \( q(t - 1) - c(t) = \sum_{j=k}^{2k} \ell_j \) only when \( q(t - 1) = \sum_{j=k}^{2k} \ell_j \) and \( c(t) = 0 \). It then follows from (13) and \( q(t - 1) - c(t) \leq \sum_{j=k}^{2k} \ell_j \) that \( \ell(t) = 1 \) only when \( q(t - 1) - c(t) = \sum_{j=k}^{2k} \ell_j \) and \( a(t) = 1 \), i.e., only when \( q(t - 1) = \sum_{j=k}^{2k} \ell_j, c(t) = 0, \) and \( a(t) = 1 \), and hence (7) holds with \( B = \sum_{j=k}^{2k} \ell_j \) at time \( t \). Thus, the maximum buffer usage property in (P3) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied at time \( t \).

**Lemma 12** Suppose that \( \ell_0^{k-1} \in A_k \), (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the ordered property in (A2) and the nonidling property in (P2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied up to time \( t - 1 \), and the circularly contiguous property in (A3) is satisfied at time \( t - 1 \). Then the ordered property in (A2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied at time \( t \).
**Proof.** We prove Lemma 12 by contradiction. Suppose that either the ordered property in (A2) or the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is not satisfied at time $t$. In the following, we divide the proof of this lemma into two parts: (i) The ordered property in (A2) is not satisfied at time $t$; (ii) The FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is not satisfied at time $t$.

(i) The ordered property in (A2) is not satisfied at time $t$. As the ordered property in (A2) is not satisfied at time $t$, it is easy to see that there are two packets in the $2k+1$ cells at time $t$ such that the earlier arrival packet is stored in a cell with a smaller index and the later arrival packet is stored in a cell with a larger index, say there exist $p_1 < p_2$ and $0 \leq i_1 < i_2 \leq 2k$ such that packet $p_1$ is stored in cell $i_1$ at time $t$ and packet $p_2$ is stored in cell $i_2$ at time $t$. As there is at most one arrival packet at any time and $p_1 < p_2$, packet $p_1$ must have arrived at the network element before time $t$ and is stored in a cell with index less than or equal to $i_1$ at time $t-1$, say packet $p_1$ is stored in cell $i_1'$ at time $t-1$ and $i_1' \leq i_1$. Since we assume that the ordered property in (A2) is satisfied at time $t-1$, it can be seen that there are only three possible cases to consider.

Case 1: Packet $p_2$ is stored in cell $i_1'$ at time $t-1$. As in this case packet $p_2$ is stored in cell $i_1'$ at time $t-1$ and is stored in cell $i_2$ at time $t$, and $i_1' \leq i_1 < i_2$, it must be the case that packet $p_2$ is stored in buffer $b_{i_1'}(0)$ at time $t-1$, switch $i_1'$ and switch $i_2$ are set to the “cross” state at time $t$, and switch $i$ is set to the “bar” state at time $t$ for $i = i_1' + 1, i_1' + 2, \ldots, i_2 - 1$, and hence packet $p_2$ is routed from the fiber delay line in cell $i_1'$ to the output link of cell $i_1'$ at time $t$ and is stored in buffer $b_{i_2}(\ell_{i_2} - 1)$ at time $t$ (see Figure 18). Since packet $p_2$ is routed from the fiber delay line in cell $i_1'$ to the output link of cell $i_1'$ at time $t$ and it is clear from $p_1 < p_2$ that packet $p_2$ is not the earliest arrival packet in cell $i_1'$ at time $t-1$, we have reached a contradiction to the FIFO departure result for cell $i_1'$ in Lemma 9 (note that we assume that the circularly contiguous property in (A3) is satisfied at time $t-1$).

Case 2: Packet $p_2$ is stored in cell $i_2'$ at time $t-1$ for some $i_2' < i_1'$. As in this case packet $p_2$ is stored in cell $i_2'$ at time $t-1$ and is stored in cell $i_2$ at time $t$, and $i_2' < i_1' \leq i_1 < i_2$, it must be the case that packet $p_2$ is stored in buffer $b_{i_2'}(0)$ at time $t-1$, switch $i_2'$ and switch $i_2$ are set to the “cross” state at time $t$, and switch $i$ is set to the “bar” state at time $t$ for $i = i_2' + 1, i_2' + 2, \ldots, i_2 - 1$, and hence packet $p_2$ is routed from the fiber delay line in cell $i_2'$ to
the output link of cell \(i_2'\) at time \(t\) and is stored in buffer \(b_{i_2}(\ell_{i_2} - 1)\) at time \(t\) (see Figure 19).

![Fig. 19. Packet \(p_2\) at time \(t\) in Case 2 of Part (i) in the proof of Lemma 12.](image)

As packet \(p_2\) is stored in cell \(i_2'\) at time \(t - 1\), it must be admitted into the network element at or before time \(t - 1\), and it follows from \(p_2 - 1 < p_2\) that packet \(p_2 - 1\) must be admitted into the network element before time \(t - 1\). As we assume that the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \(\sum_{j=k}^{2k} \ell_j\) is satisfied up to time \(t - 1\), packet \(p_1\) is stored in cell \(i_1'\) at time \(t - 1\), and \(p_2 - 1 \geq p_1\), it is easy to see that packet \(p_2 - 1\) is stored in the \(2k + 1\) cells at time \(t - 1\), say packet \(p_2 - 1\) is stored in cell \(i_1'\) at time \(t - 1\). As such, it follows from the assumption that the ordered property in (A2) is satisfied at time \(t - 1\) and \(p_1 \leq p_2 - 1 < p_2\) that \(i_2' \leq i_3' \leq i_1'\). If \(i_3' = i_2'\), then it is clear from \(p_2 - 1 < p_2\) that packet \(p_2\) is not the earliest arrival packet in cell \(i_2'\) at time \(t - 1\). Since in this case packet \(p_2\) is routed from the fiber delay line in cell \(i_2'\) to the output link of cell \(i_2'\) at time \(t\) and packet \(p_2\) is not the earliest arrival packet in cell \(i_2'\) at time \(t - 1\), we have reached a contradiction to the FIFO departure result for cell \(i_2'\) in Lemma 9. Thus, we must have

\[
i_3' > i_2'.
\] (103)

From \(i_2' + 1 \leq i_3' \leq i_1' \leq i_2' - 1\), we can see that switch \(i_3'\) and switch \(i_1'\) are set to the “bar” state at time \(t\). Therefore, packet \(p_2 - 1\) remains stored in cell \(i_3'\) at time \(t\), packet \(p_1\) remains stored in cell \(i_1'\) at time \(t\) (this implies that \(i_1' = i_1\)), and packet \(p_2\) is routed to the input link of cell \(i_3'\) at time \(t\) (see Figure 19).

We then consider the two subcases \(0 \leq i_3' \leq k - 1\) and \(k \leq i_3' \leq 2k\) separately.

**Subcase 2.1:** \(0 \leq i_3' \leq k - 1\). In this subcase, we have from \(0 \leq i_3' \leq k - 1\), \(q_{i_3'}(t - 1) \neq 0\) (note that packet \(p_2 - 1\) is stored in cell \(i_3'\) at time \(t - 1\)), and (16) that switch \(i_3'\) is set to the “cross” state at time \(t\). Since we have also shown that switch \(i_3'\) is set to the “bar” state at time \(t\), a contradiction is reached.

**Subcase 2.2:** \(k \leq i_3' \leq 2k\). As \(p_2\) is stored in cell \(i_2'\) at time \(t - 1\) and packet \(p_2 - 1\) is stored in cell \(i_3'\) at time \(t - 1\), we have

\[
q_{i_2'}(t - 1) \neq 0 \text{ and } q_{i_3'}(t - 1) \neq 0.
\] (104)

Since we assume that the ordered property in (A2) is satisfied at time \(t - 1\), we see that packet \(p_2\) is the earliest arrival packet in cell \(i_2'\) at time \(t - 1\), packet \(p_2 - 1\) is the latest arrival packet.
in cell \(i'_3\) at time \(t - 1\), and cell \(i\) is empty at time \(t - 1\) for \(i = i'_2 + 1, i'_2 + 2, \ldots, i'_3 - 1\). Thus, we have

\[
q_i(t-1) = 0, \quad \text{for } i'_2 + 1 \leq i \leq i'_3 - 1.
\] (105)

Since packet \(p_2 - 1\) is stored in cell \(i'_3\) at time \(t - 1\) and we have shown that packet \(p_2\) is routed to the input link of cell \(i'_3\) at time \(t\), we then see from Lemma 8 that packet \(p_2 - 1\) is stored in buffer \(b_{i'_3}(\ell_{i'_3} - 1)\) at time \(t - 1\) (note that the assumptions in the statement of Lemma 8 hold as we assume that the ordered property in (A2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \(\sum_{j=k}^{2k} \ell_j\) are satisfied up to time \(t - 1\)).

As we have \(k \leq i'_3 \leq 2k\), \(q_{i'_3}(t-1) \neq 0\) in (104), and switch \(i'_3\) is set to the “bar” state at time \(t\), it follows from (20) that either \(r_{i'_3}(t) = 0\) and \(\sum_{j=i'_3+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i'_3+1}^{2k} \ell_j\), or \(r_{i'_3}(t) \neq 0\) and \(r_{i'_3}(t) + q_{i'_3}(t-1) > \ell_{i'_3}\).

Subcase 2.2(a): \(r_{i'_3}(t) = 0\) and \(\sum_{j=i'_3+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i'_3+1}^{2k} \ell_j\). In this subcase, we have from \(q_{i'_3}(t-1) \neq 0\) in (104), \(r_{i'_3}(t) = 0\), and the definition of \(r_{i'_3}(t)\) that the earliest arrival packet in cell \(i'_3\) at time \(t - 1\) is stored in buffer \(b_{i'_3}(0)\) at time \(t - 1\). As \(1 \leq q_{i'_3}(t-1) \leq \ell_{i'_3}\) and we assume that the circularly contiguous property in (A3) is satisfied at time \(t - 1\), we see that the latest arrival packet in cell \(i'_3\) at time \(t - 1\) is stored in buffer \(b_{i'_3}(q_{i'_3}(t-1) - 1)\) at time \(t - 1\). Since we have shown that packet \(p_{2} - 1\) is the latest arrival packet in cell \(i'_3\) at time \(t - 1\) and it is stored in buffer \(b_{i'_3}(\ell_{i'_3} - 1)\) at time \(t - 1\), it then follows that \(q_{i'_3}(t-1) - 1 = \ell_{i'_3} - 1\), i.e.,

\[
q_{i'_3}(t-1) - 1 = \ell_{i'_3} - 1.
\] (106)

From (106) and \(\sum_{j=i'_3+1}^{2k} q_j(t-1) - c(t) = \sum_{j=i'_3+1}^{2k} \ell_j\), we have

\[
\sum_{j=i'_3}^{2k} q_j(t-1) - c(t) = q_{i'_3}(t-1) + \sum_{j=i'_3+1}^{2k} q_j(t-1) - c(t) = \ell_{i'_3} + \sum_{j=i'_3+1}^{2k} \ell_j = \sum_{j=i'_3}^{2k} \ell_j.
\] (107)

If \(i'_3 = k\), then we have from (8) and (107) that

\[
q^{(2)}(t-1) - c(t) = \sum_{j=k}^{2k} q_j(t-1) - c(t) = \sum_{j=k}^{2k} \ell_j.
\] (108)

From (108), \(q^{(2)}(t-1) \leq q(t-1)\) in (8), and \(q(t-1) \leq \sum_{j=k}^{2k} \ell_j\) in Lemma 11 (note that the assumptions in the statement of Lemma 11 hold as we assume that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer \(\sum_{j=k}^{2k} \ell_j\) is satisfied up to time \(t - 1\), we have

\[
\sum_{j=k}^{2k} \ell_j = q^{(2)}(t-1) - c(t) \leq q(t-1) - c(t) \leq \sum_{j=k}^{2k} \ell_j - c(t).
\] (109)
Since \( c(t) \) can only be 0 or 1, it is easy to see from (109) that
\[
c(t) = 0 \text{ and } q^{(2)}(t - 1) = q(t - 1) = \sum_{j=k}^{2k} \ell_j.
\]
(110)

Thus, we have from (8) that \( q^{(1)}(t - 1) = q(t - 1) - q^{(2)}(t - 1) = 0 \) and it follows that
\[
q_i(t - 1) = 0, \text{ for } 0 \leq i \leq k - 1.
\]
(111)

As we have from (103) and \( i_3' = k \) that \( i'_2 \leq i'_3 - 1 = k - 1 \), it is immediate from (111) that \( q_{i_3'}(t - 1) = 0 \), and this contradicts to \( q_{i_3'}(t - 1) \neq 0 \) in (104).

On the other hand, if \( k + 1 \leq i'_3 \leq 2k \), then we discuss the two scenarios \( i'_2 < i'_3 - 1 \) and \( i'_2 = i'_3 - 1 \) separately. When \( i'_2 < i'_3 - 1 \), we have from \( k \leq i'_3 - 1 \leq 2k - 1 \), \( q_{i'_3 - 1}(t - 1) = 0 \) in (105), (107), and (19) that switch \( i'_3 - 1 \) is set to the “cross” state at time \( t \). Since \( i'_2 + 1 \leq i'_3 - 1 \leq i'_1 - 1 = i_1 - 1 < i_2 - 1 \), we see that switch \( i'_3 - 1 \) is set to the “bar” state at time \( t \), and a contradiction is reached in this scenario. When \( i'_2 = i'_3 - 1 \), we have from \( k + 1 \leq i'_3 \leq 2k \) that \( k \leq i'_2 \leq 2k - 1 \). As packet \( p_2 \) is the earliest arrival packet in cell \( i'_3 \) at time \( t - 1 \) and packet \( p_2 \) is stored in buffer \( b_{i_2'}(0) \) at time \( t - 1 \), we see from the definition of \( r_{i_2'}(t) \) that
\[
r_{i_2'}(t) = 0.
\]
(112)

From \( k \leq i'_2 \leq 2k - 1 \), \( q_{i_3'}(t - 1) \neq 0 \) in (104), (112), (107) (note that \( i'_2 + 1 = i'_3 \)), and (20), we see that switch \( i'_2 \) is set to the “bar” state at time \( t \). Since we have already shown that switch \( i'_2 \) is set to the “cross” state at time \( t \), a contradiction is reached in this scenario.

Subcase 2.2(b): \( r_{i_3'}(t) \neq 0 \) and \( r_{i_3'}(t) + q_{i_3'}(t - 1) > \ell_{i_3'} \). As in this subcase we have \( r_{i_3'}(t) + q_{i_3'}(t - 1) > \ell_{i_3'} \), it is clear from \( r_{i_3'}(t) \leq \ell_{i_3'} - 1 \) and \( q_{i_3'}(t - 1) \leq \ell_{i_3'} \) that
\[
\ell_{i_3'} \leq r_{i_3'}(t) + q_{i_3'}(t - 1) - 1 \leq 2\ell_{i_3'} - 2.
\]
(113)

Since we assume that the circularly contiguous property in (A3) is satisfied at time \( t - 1 \), we see from (113) that the latest arrival packet in cell \( i'_3 \) at time \( t - 1 \) is stored in buffer \( b_{i_3'}((r_{i_3'}(t) + q_{i_3'}(t - 1)) \mod \ell_{i_3'}) = b_{i_3'}(r_{i_3'}(t) + q_{i_3'}(t - 1) - \ell_{i_3'} - 1) \). Since we have shown that packet \( p_2 - 1 \) is the latest arrival packet in cell \( i'_3 \) at time \( t - 1 \) and it is stored in buffer \( b_{i_3'}(\ell_{i_3'} - 1) \) at time \( t - 1 \), it then follows that \( r_{i_3'}(t) + q_{i_3'}(t - 1) - \ell_{i_3'} - 1 = \ell_{i_3'} - 1 \), and this contradicts to \( r_{i_3'}(t) + q_{i_3'}(t - 1) - \ell_{i_3'} - 1 \leq \ell_{i_3'} - 2 \) in (113).

Case 3: Packet \( p_2 \) has not arrived at the network element yet at time \( t - 1 \). As in this case packet \( p_2 \) has not arrived at the network element yet at time \( t - 1 \) and is stored in cell \( i_2 \) at time \( t \), it must be the case that packet \( p_2 \) is admitted into the network element at time \( t \), switch \( i \) is set to the “bar” state at time \( t \) for \( i = 0, 1, \ldots, i_2 - 1 \), and switch \( i_2 \) is set to the “cross” state at time \( t \), and hence packet \( p_2 \) is stored in buffer \( b_{i_2'}(\ell_{i_2'} - 1) \) at time \( t \) (see Figure 20).

Since packet \( p_2 \) is admitted into the network element at time \( t \), it follows from \( p_2 - 1 < p_2 \) that packet \( p_2 - 1 \) must be admitted into the network element before time \( t \). As we assume that
the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k}\ell_j$ is satisfied up to time $t - 1$, packet $p_1$ is stored in cell $i'_1$ at time $t - 1$, and $p_2 - 1 \geq p_1$, it is easy to see that packet $p_2 - 1$ is stored in the $2k + 1$ cells at time $t - 1$, say packet $p_2 - 1$ is stored in cell $i'_3$ at time $t - 1$, and packet $p_2 - 1$ is the latest arrival packet in the $2k + 1$ cells at time $t - 1$. It follows from the assumption that the ordered property in (A2) is satisfied at time $t - 1$ and $p_1 \leq p_2 - 1$ that $i'_3 \leq i'_1$. From $i'_3 \leq i'_1 \leq i_1 \leq i_2 - 1$, we can see that switch $i'_3$ and switch $i'_1$ are set to the “bar” state at time $t$. Therefore, packet $p_2 - 1$ remains stored in cell $i'_3$ at time $t$, packet $p_1$ remains stored in cell $i'_1$ at time $t$ (this implies that $i'_1 = i_1$), and packet $p_2$ is routed to the input link of cell $i'_3$ at time $t$ (see Figure 20).

As in Case 2 of Part (i) in the proof of Lemma 12 above, we consider the two subcases $0 \leq i'_3 \leq k - 1$ and $k \leq i'_3 \leq 2k$ separately.

Subcase 3.1: $0 \leq i'_3 \leq k - 1$. By using the same argument as in Subcase 2.1 of Part (i) in the proof of Lemma 12, a contradiction can be reached.

Subcase 3.2: $k \leq i'_3 \leq 2k$. As packet $p_2 - 1$ is stored in cell $i'_3$ at time $t - 1$, we have

\[ q_{i'_3}(t - 1) \neq 0. \]  

(114)

Since packet $p_2 - 1$ is the latest arrival packet in the $2k + 1$ cells at time $t - 1$ and we assume that the ordered property in (A2) is satisfied at time $t - 1$, we see that cell $i$ is empty at time $t - 1$ for $i = 0, 1, \ldots, i'_3 - 1$, i.e.,

\[ q_i(t - 1) = 0, \text{ for } 0 \leq i \leq i'_3 - 1. \]  

(115)

Since packet $p_2 - 1$ is stored in cell $i'_3$ at time $t - 1$ and packet $p_2$ is routed to the input link of cell $i'_3$ at time $t$, we have from Lemma 8 that packet $p_2 - 1$ is stored in buffer $b_{i'_3}(\ell_{i'_3} - 1)$ at time $t - 1$.

As we have $k \leq i'_3 \leq 2k$, $q_{i'_3}(t - 1) \neq 0$ in (114), and switch $i'_3$ is set to the “bar” state at time $t$, it follows from (20) that either $r_{i'_3}(t) = 0$ and $\sum_{j=i'_3+1}^{2k} q_j(t - 1) - c(t) = \sum_{j=i'_3+1}^{2k} \ell_j$, or $r_{i'_3}(t) \neq 0$ and $r_{i'_3}(t) + q_{i'_3}(t - 1) > \ell_{i'_3}$.

Subcase 3.2(a): $r_{i'_3}(t) = 0$ and $\sum_{j=i'_3+1}^{2k} q_j(t - 1) - c(t) = \sum_{j=i'_3+1}^{2k} \ell_j$. In this subcase, we can show as in Subcase 2.2(a) of Part (i) in the proof of Lemma 12 that (106) and (107) still hold. If $i'_3 = k$, then we can show as in Subcase 2.2(a) of Part (i) in the proof of Lemma 12 that (108)–(110) still hold. From $q(t - 1) - c(t) = \sum_{j=k}^{2k} \ell_j$ in (110) and (12), we have $a_0(t) = 0$, namely,
there is no packet admitted into the network element at time $t$. Since packet $p_2$ is admitted into the network element at time $t$, a contradiction is reached in this subcase. On the other hand, if $k + 1 \leq i'_3 \leq 2k$, then we have from $k \leq i'_3 - 1 \leq 2k - 1$, $q_{i'_3-1}(t-1) = 0$ in (115), (107), and (19) that switch $i'_3 - 1$ is set to the “cross” state at time $t$. Since we have already shown that switch $i'_3 - 1$ is set to the “bar” state at time $t$, a contradiction is reached in this subcase.

Subcase 3.2(b): $r_{i'_3}(t) \neq 0$ and $r_{i'_3}(t) + q_{i'_3}(t-1) > \ell_{i'_3}$. By using the same argument as in Subcase 2.2(b) of Part (i) in the proof of Lemma 12, a contradiction can be reached.

(ii) The FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is not satisfied at time $t$. As the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is not satisfied at time $t$, it is easy to see that there are two packets such that the earlier arrival packet is stored in the $2k + 1$ cells at time $t$ and the later arrival packet departs from the departure link of the network element at time $t$, say there exist $p_1 < p_2$ such that packet $p_1$ is stored in cell $i_1$ at time $t$ for some $0 \leq i_1 \leq 2k$ and packet $p_2$ is routed to the departure link of the network element at time $t$. As there is at most one arrival packet at any time and $p_1 < p_2$, packet $p_1$ must have arrived at the network element before time $t$ and is stored in a cell with index less than or equal to $i_1$ at time $t - 1$, say packet $p_1$ is stored in cell $i'_1$ at time $t - 1$ and $i'_1 \leq i_1$. Since the ordered property in (A2) is satisfied at time $t - 1$, it can be seen that there are only three possible cases to consider.

Case 1: Packet $p_2$ is stored in cell $i'_1$ at time $t - 1$. As packet $p_2$ is routed to the departure link of the network element at time $t$, it must be the case that packet $p_2$ is stored in buffer $b_{i'_1}(0)$ at time $t - 1$, switch $i'_1$ is set to the “cross” state at time $t$, and switch $i$ is set to the “bar” state at time $t$ for $i = i'_1 + 1, i'_1 + 2, \ldots, 2k$, and hence packet $p_2$ is routed from the fiber delay line in cell $i'_1$ to the output link of cell $i'_1$ at time $t$ and is routed to the departure link of the network element at time $t$ (see Figure 21). Since it is clear from $p_1 < p_2$ that packet $p_2$ is not the earliest arrival packet in cell $i'_1$ at time $t - 1$, we have reached a contradiction to the FIFO departure result for cell $i'_1$ in Lemma 9.

Case 2: Packet $p_2$ is stored in cell $i'_2$ at time $t - 1$ for some $i'_2 < i'_1$. As packet $p_2$ is routed to the departure link of the network element at time $t$, it must be the case that packet $p_2$ is stored in buffer $b_{i'_2}(0)$ at time $t - 1$, switch $i'_2$ is set to the “cross” state at time $t$, and switch $i$ is set to the “bar” state at time $t$ for $i = i'_2 + 1, i'_2 + 2, \ldots, 2k$, and hence packet $p_2$ is routed from the

![Fig. 21. Packet $p_2$ at time $t$ in Case 1 of Part (ii) in the proof of Lemma 12.](image-url)
fiber delay line in cell \( i'_2 \) to the output link of cell \( i'_2 \) at time \( t \) and is routed to the departure link of the network element at time \( t \) (see Figure 22).

As in Case 2 of Part (i) in the proof of Lemma 12 above, we can show that packet \( p_2 - 1 \) is stored in the \( 2k + 1 \) cells at time \( t - 1 \), say packet \( p_2 - 1 \) is stored in cell \( i'_3 \) at time \( t - 1 \). It follows from the assumption that the ordered property in \( (A2) \) is satisfied at time \( t - 1 \) and \( p_1 \leq p_2 - 1 < p_2 \) that \( i'_2 \leq i'_3 \leq i'_1 \). If \( i'_3 = i'_2 \), then it is clear from \( p_2 - 1 < p_2 \) that packet \( p_2 \) is not the earliest arrival packet in cell \( i'_2 \) at time \( t - 1 \). Since in this case packet \( p_2 \) is routed from the fiber delay line in cell \( i'_2 \) to the output link of cell \( i'_2 \) at time \( t \) and packet \( p_2 \) is not the earliest arrival packet in cell \( i'_2 \) at time \( t - 1 \), we have reached a contradiction to the FIFO departure result for cell \( i'_2 \) in Lemma 9. Thus, we must have \( i'_3 > i'_2 \) as in (103). Therefore, we see from \( i'_2 + 1 \leq i'_3 \leq 2k \) that switch \( i'_3 \) is set to the “bar” state at time \( t \) and packet \( p_2 \) is routed to the input link of cell \( i'_3 \) at time \( t \) (see Figure 22).

It should be clear that the difference between Case 2 of Part (i) and Case 2 of Part (ii) in the proof of Lemma 12 is as follows: In Case 2 of Part (i) in the proof of Lemma 12, switch \( i \) is set to the “bar” state at time \( t \) for \( i = i'_2 + 1, i'_2 + 2, \ldots, i'_2 - 1 \) and switch \( i_2 \) is set to the “cross” state at time \( t \) so that packet \( p_2 \) is stored in buffer \( b_{i_2} (i'_2 - 1) \) at time \( t \); however, in Case 2 of Part (ii) in the proof of Lemma 12, switch \( i \) is set to the “bar” state at time \( t \) for \( i = i'_2 + 1, i'_2 + 2, \ldots, 2k \) so that packet \( p_2 \) is routed to the departure link of the network element at time \( t \). Therefore, by considering the two subcases \( 0 \leq i'_3 \leq k - 1 \) and \( k \leq i'_3 \leq 2k \) separately and using the same argument as in Case 2 of Part (i) in the proof of Lemma 12, a contradiction can be reached in this case.

Case 3: Packet \( p_2 \) has not arrived at the network element yet at time \( t - 1 \). As packet \( p_2 \) is stored in cell \( i'_2 \) at time \( t \), it must be the case that packet \( p_2 \) is admitted into the network element at time \( t \) and switch \( i \) is set to the “bar” state at time \( t \) for \( i = 0, 1, \ldots, 2k \), and hence packet \( p_2 \) is routed to the departure link of the network element at time \( t \) (see Figure 23).

As in Case 3 of Part (i) in the proof of Lemma 12 above, we can show that packet \( p_2 - 1 \) is stored in the \( 2k + 1 \) cells at time \( t - 1 \), say packet \( p_2 - 1 \) is stored in cell \( i'_3 \) at time \( t - 1 \), and packet \( p_2 - 1 \) is the latest arrival packet in the \( 2k + 1 \) cells at time \( t - 1 \). Therefore, switch \( i'_3 \) is set to the “bar” state at time \( t \) and packet \( p_2 \) is routed to the input link of cell \( i'_3 \) at time \( t \) (see Figure 22).
Figure 23). It should also be clear that by considering the two subcases $0 \leq i'_{3} \leq k - 1$ and $k \leq i'_{3} \leq 2k$ separately and using the same argument as in Case 3 of Part (i) in the proof of Lemma 12, a contradiction can be reached in this case.

**Lemma 13** Suppose that $\ell_{0}^{k-1} \in A_{k}$, (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the ordered property in (A2) and the nonidling property in (P2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_{j}$ are satisfied up to time $t - 1$, and the circularly contiguous property in (A3) is satisfied at time $t - 1$. Then the circularly contiguous property in (A3) is satisfied at time $t$.

**Proof.** Let $0 \leq i \leq 2k$ and consider cell $i$ at time $t$. If there is at most one packet in cell $i$ at time $t$, then it is clear that the circularly contiguous property in (A3) holds at time $t$. As $q_{i}(t) \leq \ell_{i} = 1$ for $i = 0$ or $i = 2k$, we assume without loss of generality that $1 \leq i \leq 2k - 1$ and $2 \leq q_{i}(t) \leq \ell_{i}$ in the rest of the proof.

Note that from the assumptions in the statement of this lemma, we can see that the assumptions in the statements of Lemma 2, Lemma 8, Lemma 9, and Lemma 12 hold. From Lemma 12, we see that the ordered property in (A2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_{j}$ are satisfied at time $t$. It then follows that the assumptions in the statement of Lemma 10 also hold.

From (22), $a_{i}(t)$ and $d_{i}(t)$ can only be 0 or 1, and $q_{i}(t) \geq 2$, we can see that

$$q_{i}(t - 1) = q_{i}(t) + d_{i}(t) - a_{i}(t) \geq q_{i}(t) - 1 \geq 1.$$  \hspace{1cm} (116)

Thus, cell $i$ is nonempty at time $t - 1$. We then consider the two cases $a_{i}(t) = 0$ and $a_{i}(t) = 1$ separately.

**Case 1:** $a_{i}(t) = 0$, i.e., there is no packet routed to the input link of cell $i$ at time $t$. Let packet $p$ be the “earliest” arrival packet in cell $i$ at time $t - 1$. As the circularly contiguous property in (A3) is satisfied at time $t - 1$, we see that packet $p + j$ is stored in buffer $b_{i}((r_{i}(t) + j) \mod \ell_{i})$ at time $t - 1$ for $j = 0, 1, \ldots, q_{i}(t - 1) - 1$. It is easy to see that if packet $p + j$ is still
stored in cell \( i \) at time \( t \) for some \( 0 \leq j \leq q_i(t-1) - 1 \), then it must be stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \). To see this, assume that packet \( p + j \) is still stored in cell \( i \) at time \( t \) for some \( 0 \leq j \leq q_i(t-1) - 1 \). If \( (r_i(t) + j) \mod \ell_i = 0 \), then packet \( p + j \) is stored in buffer \( b_i(0) \) at time \( t - 1 \) and hence switch \( i \) must be set to the “bar” state at time \( t \) so that packet \( p + j \) can be routed into the fiber delay line in cell \( i \) at time \( t \) and be stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \). On the other hand, if \( (r_i(t) + j) \mod \ell_i \neq 0 \), then it is clear that packet \( p + j \) is stored in buffer \( b_i([((r_i(t) + j) \mod \ell_i) - 1) = b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \) no matter switch \( i \) is set to the “cross” state or the “bar” state at time \( t \).

We need to consider the following two possible subcases.

Subcase I(a): Switch \( i \) is set to the “cross” state at time \( t \). If \( r_i(t) = 0 \), then it is clear that packet \( p \) is stored in buffer \( b_i(0) \) at time \( t - 1 \). Thus, it is easy to see that packet \( p \) is routed to the output link of cell \( i \) at time \( t \), packet \( p + j \) is stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \) for \( j = 1, 2, \ldots, q_i(t-1) - 1 \) (as packet \( p + j \) is still stored in cell \( i \) at time \( t \) for \( j = 1, 2, \ldots, q_i(t-1) - 1 \), and there is no packet routed into the fiber delay line in cell \( i \) at time \( t \) (as there is no packet routed to the input link of cell \( i \) at time \( t \)) (see (i) and (ii) in Figure 24(a)). As such, we have \( d_i(t) = 1 \) and it then follows from (22) and \( a_i(t) = 0 \) that

\[
q_i(t) = q_i(t-1) + a_i(t) - d_i(t) = q_i(t-1) - 1. \tag{117}
\]

As we have from (117) and \( q_i(t) \geq 2 \) that \( q_i(t-1) = q_i(t) + 1 \geq 3 \), it is clear that packet \( p + 1 \) is stored in cell \( i \) at time \( t \) and it is the earliest arrival packet in cell \( i \) at time \( t \). Since packet \( p + 1 \) is stored in buffer \( b_i(r_i(t) \mod \ell_i) \) at time \( t \), we have from the definition of \( r_i(t+1) \) that \( r_i(t+1) = (r_i(t) \mod \ell_i) \). Therefore, since packet \( p + j \) is stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \) for \( j = 1, 2, \ldots, q_i(t-1) - 1 \), we see from \( r_i(t+1) = (r_i(t) \mod \ell_i) \) and \( q_i(t) = q_i(t-1) - 1 \) in (117) that packet \( p + 1 + j \) is stored in buffer \( b_i((r_i(t) + j) \mod \ell_i)) = b_i((r_i(t+1)+j) \mod \ell_i) \) at time \( t \) for \( j = 0, 1, \ldots, q_i(t-1) - 2 = q_i(t) - 1 \) (see (iii) in Figure 24(a)). In other words, the circularly contiguous property in (A3) is satisfied at time \( t \) in this subcase.

On the other hand, if \( r_i(t) \neq 0 \), then we have \( r_i(t) + q_i(t-1) \leq \ell_i \). We prove this by contradiction. Suppose that \( r_i(t) + q_i(t-1) > \ell_i \). It is clear that packet \( p + \ell_i - r_i(t) \) is stored in \( b_i(0) \) at time \( t - 1 \) and we have from \( r_i(t) \neq 0 \) that it is not the earliest arrival packet in cell \( i \) at time \( t - 1 \). It follows that packet \( p + \ell_i - r_i(t) \) is routed to the output link of cell \( i \) at time \( t \), and this contradicts to the FIFO departure result for cell \( i \) in Lemma 9. Hence, we see from \( r_i(t) \neq 0, r_i(t) + q_i(t-1) \leq \ell_i \), and Lemma 2(i) that buffer \( b_i(0) \) is empty at time \( t - 1 \). Thus, it is easy to see that packet \( p + j \) is stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \) for \( j = 0, 1, \ldots, q_i(t-1) - 1 \) (as packet \( p + j \) is still stored in cell \( i \) at time \( t \) for \( j = 0, 1, \ldots, q_i(t-1) - 1 \), there is no packet routed into the fiber delay line in cell \( i \) at time \( t \) (as there is no packet routed to the input link of cell \( i \) at time \( t \)), and there is no packet routed to the output link of cell \( i \) at time \( t \) (as buffer \( b_i(0) \) is empty at time \( t - 1 \)).
At time $t$ (i) At time $t-1$

\begin{align*}
(i) & \quad \begin{array}{c}
\text{Subcase 1(b): Switch } i \text{ is set to the "bar" state at time } t. \text{ In this subcase, it is easy to see that packet } p+j \text{ is stored in buffer } b_i((r_i(t)+j-1) \mod \ell_i) \text{ at time } t \text{ for } j = 0, 1, \ldots, q_i(t-1) - 1 \text{ (as packet } p+j \text{ is still stored in cell } i \text{ at time } t \text{ for } j = 0, 1, \ldots, q_i(t-1) - 1), \text{ and there is no packet routed to the output link of cell } i \text{ at time } t \text{ (as there is no packet routed to the input link of cell } i \text{ at time } t) \text{ (see (i) and (ii) in Figure 25(a) and Figure 25(b)). Thus, we have } d_i(t) = 0 \text{ and it then follows from (22) and } a_i(t) = 0 \text{ that } q_i(t) = q_i(t-1) + a_i(t) - d_i(t) = q_i(t-1). \end{align*}
As it is clear that packet $p$ is still the earliest arrival packet in cell $i$ at time $t$ and it is stored in buffer $b_i \left( (r_i(t-1) \mod \ell_i) \right)$ at time $t$, we have from the definition of $r_i(t+1)$ that $r_i(t+1) = ( (r_i(t) - 1) \mod \ell_i ).$ Therefore, since packet $p+j$ is stored in buffer $b_i \left( (r_i(t) + j - 1) \mod \ell_i \right)$ at time $t$ for $j = 0, 1, \ldots, q_i(t-1) - 1$, we see from $r_i(t+1) = ( (r_i(t) - 1) \mod \ell_i \right)$ and $q_i(t) = q_i(t-1)$ that packet $p+j$ is stored in $b_i \left( (r_i(t) + j - 1) \mod \ell_i \right) = b_i \left( (r_i(t+1) + j) \mod \ell_i \right)$ at time $t$ for $j = 0, 1, \ldots, q_i(t-1) - 1 = q_i(t-1)$ (see (iii) in Figure 25(a) and Figure 25(b)). In other words, the circularly contiguous property in (A3) is satisfied at time $t$ in this subcase.

Case 2: $a_i(t) = 1$, i.e., there is a packet routed to the input link of cell $i$ at time $t$. Let packet $p'$ be the “latest” arrival packet in cell $i$ at time $t-1$. As packet $p'$ is the latest arrival packet in cell $i$ at time $t-1$ and in this case there is a packet routed to the input link of cell $i$ at time $t$, we have from Lemma 10 that the packet routed to the input link of cell $i$ at time $t$ is packet $p'+1$, and hence we have from Lemma 8 that packet $p'$ is stored in buffer $b_i \left( \ell_i - 1 \right)$ at time $t-1$. Since we assume that the circularly contiguous property in (A3) is satisfied at time $t-1$, it then follows that packet $p' - j$ is stored in buffer $b_i \left( \ell_i - 1 - j \right)$ at time $t-1$ for $0 \leq j \leq q_i(t-1) - 1$.

In this case, switch $i$ must be set to the “cross” state at time $t$. We prove this by contradiction. Suppose that switch $i$ is set to the “bar” state at time $t$. As packet $p'$ is stored in cell $i$ at time
t − 1 and switch i is set to the “bar” state at time t, it is clear that packet p′ is still stored in cell i at time t. Since we have shown that packet p′ + 1 is routed to the input link of cell i at time t, it is easy to see that packet p′ + 1 is either stored in buffer b_i(ℓ_i − 1) at time t for some i < i′ ≤ 2k or routed to the departure link of the network element at time t. If packet p′ + 1 is stored in buffer b_i(ℓ_i − 1) at time t for some i < i′ ≤ 2k, then the ordered property in (A2) is not satisfied at time t (as packet p′ is stored in cell i at time t), and we have reached a contradiction. On the other hand, if packet p′ + 1 is routed to the departure link of the network element at time t, then the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is not satisfied at time t (as packet p′ is stored in cell i at time t − 1 and hence packet p′ + 1 is not the earliest arrival packet stored in cell i at time t − 1), and we have also reached a contradiction.

Note that the “earliest” arrival packet in cell i at time t − 1 is packet p′ − q_i(t − 1) + 1 and it is stored in in buffer b_i(ℓ_i − q_i(t − 1)) at time t − 1. Let p = p′ − q_i(t − 1) + 1. Then we see that packet p is the “earliest” arrival packet in cell i at time t − 1 and we have from the definition of \( r_i(t) \) that \( r_i(t) = \ell_i - q_i(t - 1) \). As such, we see that packet p + j is stored in buffer b_i((r_i(t) + j) \mod \ell_i) at time t for j = 0, 1, …, q_i(t − 1) − 1, and packet p + q_i(t − 1) is routed to the input link of cell i at time t. As we have from (116) that 1 ≤ q_i(t − 1) ≤ \ell_i, we then consider the two cases 1 ≤ q_i(t − 1) < \ell_i and q_i(t − 1) = \ell_i separately.

Subcase 2(a): 1 ≤ q_i(t − 1) < \ell_i. In this subcase, we have r_i(t) = \ell_i - q_i(t - 1) > 0. It then follows from r_i(t) \neq 0, r_i(t) + q_i(t − 1) = \ell_i, and Lemma 2(i) that buffer b_i(0) is empty at time t − 1. As we have shown that switch i is set to the “cross” state at time t, it is easy to see that packet p + j is stored in buffer b_i((r_i(t) + j − 1) \mod \ell_i) at time t for j = 0, 1, …, q_i(t − 1) − 1 (as packet p + j is still stored in cell i at time t for j = 0, 1, …, q_i(t − 1) − 1), packet p + q_i(t − 1) is routed into the fiber delay line in cell i at time t and is stored in buffer b_i(\ell_i - 1) = b_i((r_i(t) + q_i(t − 1) − 1) \mod \ell_i) at time t (note that r_i(t) = \ell_i - q_i(t - 1)), and there is no packet routed to the output link of cell i at time t (as buffer b_i(0) is empty at time t − 1) (see (i) and (ii) in Figure 26(a)). As such, we have d_i(t) = 0 and it then follows from (22) and \( a_i(t) = 1 \)

\[
q_i(t) = q_i(t - 1) + a_i(t) - d_i(t) = q_i(t - 1) + 1.
\]

As it is clear that packet p is still the earliest arrival packet in cell i at time t and it is stored in buffer b_i((r_i(t − 1) \mod \ell_i) at time t, we have from the definition of r_i(t + 1) that \( r_i(t + 1) = ((r_i(t) - 1) \mod \ell_i). \) Therefore, since packet p + j is stored in buffer b_i((r_i(t) + j − 1) \mod \ell_i) at time t for j = 0, 1, …, q_i(t − 1), we see from r_i(t + 1) = ((r_i(t) − 1) \mod \ell_i) and \( q_i(t) = q_i(t - 1) + 1 \) in (119) that packet p + j is stored in buffer b_i((r_i(t) + j − 1) \mod \ell_i) = b_i((r_i(t + 1) + j) \mod \ell_i) at time t for j = 0, 1, …, q_i(t − 1) = q_i(t - 1) (see (iii) in Figure 26(a)). In other words, the circularly contiguous property in (A3) is satisfied at time t in this subcase.

Subcase 2(b): \( q_i(t − 1) = \ell_i \). In this subcase, we have r_i(t) = \ell_i - q_i(t - 1) = 0 and hence packet p is stored in buffer b_i(0) at time t − 1. As switch i is set to the “cross” state at time t, it
At time \( t-1 \) packet \( p+1 \) is stored in cell \( i \). It is easy to see that packet \( p \) is routed to the output link of cell \( i \) at time \( t \), packet \( p+j \) is stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \) for \( j = 1, 2, \ldots, q_i(t-1) - 1 \) (as packet \( p+j \) is still stored in cell \( i \) at time \( t \) for \( j = 1, 2, \ldots, q_i(t-1) - 1 \), and packet \( p + q_i(t-1) \) is stored in buffer \( b_i((r_i(t) + q_i(t-1) - 1) \mod \ell_i) \) at time \( t \) (see (i) and (ii) in Figure 26(b)). As such, we have \( d_i(t) = 1 \) and it then follows from (22) and \( a_i(t) = 1 \) that

\[
q_i(t) = q_i(t-1) + a_i(t) - d_i(t) = q_i(t-1) + 1.
\]

As we have from (120) and \( q_i(t) \geq 2 \) that \( q_i(t-1) = q_i(t) \geq 2 \), it is clear that packet \( p+1 \) is stored in cell \( i \) at time \( t \) and it is the earliest arrival packet in cell \( i \) at time \( t \). Since packet \( p+1 \) is stored in buffer \( b_i(r_i(t) \mod \ell_i) \) at time \( t \), we have from the definition of \( r_i(t+1) \) that

\[
r_i(t+1) = (r_i(t) \mod \ell_i).
\]

Therefore, since packet \( p+j \) is stored in buffer \( b_i((r_i(t) + j - 1) \mod \ell_i) \) at time \( t \) for \( j = 1, 2, \ldots, q_i(t-1) \), we see from \( r_i(t+1) = (r_i(t) \mod \ell_i) \) and \( q_i(t) = q_i(t-1) \) in (120) that packet \( (p+1)+j \) is stored in buffer \( b_i((r_i(t) + j) \mod \ell_i) = b_i((r_i(t+1) + j) \mod \ell_i) \) at time \( t \) for \( j = 0, 1, \ldots, q_i(t-1) - 1 = q_i(t-1) \) (see (iii) in Figure 26(b)). In other words, the circularly contiguous property in (A3) is satisfied at time \( t \) in this subcase.
Lemma 14 Suppose that $e_{0}^{k-1} \in \mathcal{A}_{k}$, (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Also suppose that the ordered property in (A2), the circularly contiguous property in (A3), and the nonidling property in (P2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=1}^{2k} \ell_{j}$ are satisfied up to time $t - 1$. Then the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer $\sum_{j=1}^{2k} \ell_{j}$ is satisfied at time $t$.

Proof. Note that from the assumptions in the statement of this lemma, we can see that the assumptions in the statements of Lemma 6, Lemma 8, and Lemma 12 hold. From Lemma 12, we see that the ordered property in (A2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=1}^{2k} \ell_{j}$ are satisfied at time $t$. It then follows that the assumptions in the statements of Lemma 10 also hold.

To show that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer $\sum_{j=1}^{2k} \ell_{j}$ is satisfied at time $t$, we need to show that (6) holds, i.e., if $c(t) = 1$ and $q(t-1)+a(t) > 0$, then $d(t) = 1$; otherwise $d(t) = 0$. We consider the following three possible cases.

Case 1: $c(t) = 0$. In this case, we have $c(t) = 0$ and hence we need to show that $d(t) = 0$. It is clear that

$$\sum_{j=2k+1}^{2k} q_{j}(t-1) - c(t) = 0 = \sum_{j=2k+1}^{2k} \ell_{j}.$$ (121)

Note that $0 \leq q_{2k}(t-1) \leq \ell_{2k} = 1$. If $q_{2k}(t-1) = 0$, then we see from (121) and (19) that switch $2k$ is set to the “cross” state at time $t$. As there is no packet stored in cell $2k$ at time $t - 1$, it is easy to see that there is no packet routed to the output link of cell $2k$ at time $t$, i.e., there is no packet routed to the departure link of the network element at time $t$, and hence we have $d(t) = 0$.

On the other hand, if $q_{2k}(t-1) = 1$, then the packet stored in cell $2k$ at time $t - 1$ is stored in buffer $b_{2k}(0)$ (as buffer $b_{2k}(0)$ is only buffer in cell $2k$) and it is the earliest arrival packet in the $2k+1$ cells at time $t - 1$ (as we assume that the ordered property in (A2) is satisfied at time $t - 1$). It is clear from the definition of $r_{2k}(t)$ that $r_{2k}(t) = 0$. From $q_{2k}(t-1) = 1$, $r_{2k}(t) = 0$, (121), and (20), we see that switch $2k$ is set to the “bar” state at time $t$. Thus, the packet stored in cell $2k$ at time $t - 1$ is still stored in cell $2k$ at time $t$, i.e., the earliest arrival packet in the $2k+1$ cells at time $t - 1$ is still stored in the $2k+1$ cells at time $t$. Since the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=1}^{2k} \ell_{j}$ is satisfied at time $t$, it then follows that there is no packet routed to the departure link of the network element at time $t$, and hence we have $d(t) = 0$.

Case 2: $c(t) = 1$ and $q(t-1) = 0$. If $a(t) = 0$, then we have $c(t) = 1$ and $q(t-1)+a(t) = 0$ and hence we need to show that $d(t) = 0$. As there is no packet stored in the $2k+1$ cells at time $t - 1$ and there is no arrival packet from the arrival link of the network element at time $t$,
it is clear that there is no packet routed to the departure link of the network element at time $t$, and hence we have $d(t) = 0$.

On the other hand, if $a(t) = 1$, then we have $c(t) = 1$ and $q(t - 1) + a(t) > 0$ and hence we need to show that $d(t) = 1$. As $q(t - 1) - c(t) = -1 < \sum_{j=k}^{2k} \ell_j$, we have from (12) that $a_0(t) = a(t) = 1$, i.e., the arrival packet from the arrival link of the network element at time $t$ is admitted into the network element at time $t$.

Since $q(t - 1) = 0$, it is clear from (8) that

$$q_i(t - 1) = 0, \text{ for } 0 \leq i \leq 2k,$$

and $q^{(1)}(t - 1) = 0$ and $q^{(2)}(t - 1) = 0$.  \hspace{1cm} (122)

From (123), we see that the cell index $j(t)$ as defined in (14) is given by

$$j(t) = 2k.$$  \hspace{1cm} (124)

From (124), $q_{2k}(t - 1) = 0$ in (122), and the definition of $w_{2k}(t)$, we have

$$w_{j(t)}(t) = w_{2k}(t) = 0.$$  \hspace{1cm} (125)

Furthermore, from (122) and $c(t) = 1$, we have

$$\sum_{j=i+1}^{2k} q_j(t - 1) - c(t) = -1 < \sum_{j=i+1}^{2k} \ell_j, \text{ for } 0 \leq i \leq 2k.$$  \hspace{1cm} (126)

Thus, we see from $q^{(1)}(t - 1) = 0$ in (123), (125), and (15) that switch $i$ is set to the “bar” state at time $t$ for $i = 0, 1, \ldots, k - 1$, and we see from (122), (126), and (19) that switch $i$ is set to the “bar” state at time $t$ for $i = k, k + 1, \ldots, 2k$. Therefore, the packet admitted into the network element at time $t$ is routed to the departure link of the network element at time $t$ (see Figure 27), and hence we have $d(t) = 1$.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{fig27}
\caption{The arrival packet from the arrival link of network element at time $t$ in Case 2 in the proof of Lemma 14.}
\end{figure}

Case 3: $c(t) = 1$ and $q(t - 1) \neq 0$. In this case, we have $c(t) = 1$ and $q(t - 1) + a(t) \geq q(t - 1) > 0$, and we need to show that $d(t) = 1$. Let

$$i_1 = \max\{0 \leq i \leq 2k : q_i(t - 1) \neq 0\}.$$  \hspace{1cm} (127)
Note that \( i_1 \) is well defined as in this case we have \( q(t - 1) \neq 0 \). It is clear from the definition of \( i_1 \) in (127) that
\[
q_{i_1}(t - 1) \neq 0, \quad (128)
\]
\[
q_i(t - 1) = 0, \text{ for } i_1 + 1 \leq i \leq 2k. \quad (129)
\]

From (129) and \( c(t) = 1 \), we have
\[
\sum_{j=1+1}^{2k} q_j(t - 1) - c(t) = -1 < \sum_{j=1+1}^{2k} \ell_j, \text{ for } i_1 \leq i \leq 2k. \quad (130)
\]

As \( q(t - 1) \neq 0 \), there is at least one packet stored in the \( 2k + 1 \) cells at time \( t - 1 \). Let packet \( p \) be the earliest arrival packet in the \( 2k + 1 \) cells at time \( t - 1 \). As we assume that the ordered property in (A2) is satisfied at time \( t - 1 \), it is clear from the definition of \( i_1 \) in (127) that packet \( p \) is stored in cell \( i_1 \) at time \( t - 1 \). We then consider the three subcases \( 0 \leq i_1 \leq k - 1, k \leq i_1 < 2k \), and \( i_1 = 2k \) separately.

Subcase 3.1: \( 0 \leq i_1 \leq k - 1 \). Assume that packet \( p \) arrives at the network element at time \( t_0 \). As packet \( p \) is stored in cell \( i_1 \) at time \( t - 1 \), it is clear that \( t_0 \leq t - 1 \). Since packet \( p \) arrives at the network element at time \( t_0 \), it is clear that packet \( p - 1 \) arrives at the network element at or before time \( t_0 - 1 \). Furthermore, since packet \( p - 1 \) arrives at the network element at or before time \( t_0 - 1 \), packet \( p \) is the earliest arrival packet in the \( 2k + 1 \) cells at time \( t - 1 \), and \( t_0 - 1 < t - 1 \), it is easy to see that packet \( p - 1 \) has departed from the network element by time \( t - 1 \). We then consider the following three possible subcases for packet \( p - 1 \).

Subcase 3.1(a): Packet \( p - 1 \) is stored in cell \( i_2 \) at time \( t_0 - 1 \) for some \( 0 \leq i_2 \leq k - 1 \). In this subcase, it is clear that packet \( p - 1 \) is the latest arrival packet in the \( 2k + 1 \) cells at time \( t_0 - 1 \) as packet \( p \) has not arrived at the network element yet at time \( t_0 - 1 \). Since packet \( p - 1 \) is stored in the first \( k \) cells at time \( t_0 - 1 \) and is not stored in the first \( k \) cells at time \( t - 1 \) (as packet \( p - 1 \) has departed from the network element by time \( t - 1 \)), it then follows from Lemma 6(iii) that packet \( p - 1 \) and packet \( p \) are routed to the output link of cell \( k - 1 \) consecutively at or before time \( t \), say at time \( t' - 1 \) and time \( t' \) with \( t' \leq t \), respectively. As packet \( p \) is stored in cell \( i_1 \) at time \( t - 1 \) and is routed to the output link of cell \( k - 1 \) at time \( t' \), and \( 0 \leq i_1 \leq k - 1 \), it is also easy to see that \( t' > t - 1 \). From \( t' \leq t \) and \( t' > t - 1 \), we see that \( t' = t \). Thus, packet \( p \) is routed to the output link of cell \( k - 1 \) at time \( t \). From \( 0 \leq i_1 \leq k - 1 \), (129), (130), and (19), we see that switch \( i \) is set to the “bar” state at time \( t \) for \( i = k, k + 1, \ldots, 2k \). Therefore, packet \( p \) is routed to the departure link of the network element at time \( t \), and hence we have \( d(t) = 1 \).

Subcase 3.1(b): Packet \( p - 1 \) is stored in cell \( i_2 \) at time \( t_0 - 1 \) for some \( k \leq i_2 \leq 2k \). In this subcase, it is also clear that packet \( p - 1 \) is the latest arrival packet in the \( 2k + 1 \) cells at time \( t_0 - 1 \) as packet \( p \) has not arrived at the network element yet at time \( t_0 - 1 \). Since packet \( p - 1 \) is stored in the last \( k + 1 \) cells at time \( t_0 - 1 \), it follows from Lemma 6(ii) that packet \( p \) is routed
to the output link of cell $k-1$ at time $t_0 + w_{i_2}(t_0)$. As packet $p$ is stored in cell $i_1$ at time $t-1$ and $0 \leq i_1 \leq k-1$, it is clear that

$$t_0 + w_{i_2}(t_0) > t - 1.$$  \hspace{1cm} (131)

If $w_{i_2}(t_0) = 0$, then we have from (131) that $t_0 > t - 1$. As we also have $t_0 \leq t - 1$, a contradiction is reached. It follows that we must have $w_{i_2}(t_0) \neq 0$. Since packet $p - 1$ is the latest arrival packet in the $2k + 1$ cells at time $t_0 - 1$, it is also the latest arrival packet in cell $i_2$ at time $t_0 - 1$. We then see from $w_{i_2}(t_0) \neq 0$ and (10) that packet $p - 1$ is stored in buffer $b_{i_2}(w_{i_2}(t_0) - 1)$ at time $t_0 - 1$, and hence it is stored in buffer $b_{i_2}(0)$ at time $t_0 + w_{i_2}(t_0) - 2$. As packet $p - 1$ is stored in cell $i_2$ at time $t_0 + w_{i_2}(t_0) - 2$ and packet $p - 1$ has departed from the network element by time $t - 1$, it is easy to see that

$$t_0 + w_{i_2}(t_0) - 2 < t - 1.$$  \hspace{1cm} (132)

From (131) and (132), we have $t_0 + w_{i_2}(t_0) = t$. As such, packet $p$ is routed to the output link of cell $k-1$ at time $t_0 + w_{i_2}(t_0) = t$. From $0 \leq i_1 \leq k-1$, (129), (130), and (19), we see that switch $i$ is set to the “bar” state at time $t$ for $i = k, k+1, \ldots, 2k$. Therefore, packet $p$ is routed to the departure link of the network element at time $t$, and hence we have $d(t) = 1$.

**Subcase 3.1(c): Packet $p - 1$ has departed from the network element by time $t_0 - 1$.** As packet $p - 1$ has departed from the network element by time $t_0 - 1$ and we assume that the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied up to time $t_0 - 1$ (note that $t_0 - 1 < t - 1$), it is easy to see that packets admitted into the network element earlier than packet $p - 1$ have also departed from the network element by time $t_0 - 1$. Since packet $p$ arrives at the network element at time $t_0$, it is clear that packets admitted into the network element later than packet $p - 1$ have not arrived at the network element yet at time $t_0 - 1$. As such, we can see that the $2k + 1$ cells are empty at time $t_0 - 1$, i.e., $q(t_0 - 1) = 0$.

It follows from $q(t_0 - 1) = 0$ that (122)–(125) hold with $t$ replaced by $t_0$. Thus, we see from $q^{(1)}(t_0 - 1) = 0$ in (123), $w_j(t_0) = 0$ in (125), and (15) that switch $i$ is set to the “bar” state at time $t_0$ for $i = 0, 1, \ldots, k - 1$. As packet $p$ is admitted into the network element at time $t_0$, we then see that packet $p$ is routed to the output link of cell $k - 1$ at time $t_0$. As packet $p$ is stored in cell $i_1$ at time $t - 1$ and $0 \leq i_1 \leq k - 1$, we must have $t_0 > t - 1$. Since we also have $t_0 \leq t - 1$, a contradiction is reached. Therefore, this subcase cannot happen.

**Subcase 3.2: $k \leq i_1 < 2k$.** As packet $p$ is the earliest arrival packet in the $2k + 1$ cells at time $t - 1$, it is also the earliest arrival packet in cell $i_1$ at time $t - 1$. We claim that packet $p$ is stored in buffer $b_{i_1}(0)$ at time $t - 1$. We show this claim by contradiction. Suppose that packet $p$ is stored in buffer $b_{i_1}(j_1)$ at time $t - 1$ for some $1 \leq j_1 \leq \ell_{i_1} - 1$. It is clear that packet $p$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1)$ at time $t + j_1 - \ell_{i_1}$.

We first prove by contradiction that packet $p$ is also the earliest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1}$. Assume that packet $p$ is not the earliest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1}$,
As we assume that the circularly contiguous property in (A3) is satisfied at time \( t + j_1 - \ell_{i_1} \) (note that \( t + j_1 - \ell_{i_1} \leq t - 1 \)), it is clear that packet \( p - 1 \) is also stored in cell \( i_1 \) at time \( t + j_1 - \ell_{i_1} \) and it is stored in buffer \( b_{i_1}(\ell_{i_1} - 2) \) at time \( t + j_1 - \ell_{i_1} \). Therefore, packet \( p - 1 \) is stored in buffer \( b_{i_1}(j_1 - 1) \) at time \( t - 1 \) (note that \( j_1 \geq 1 \)), and this contradicts to the assumption that packet \( p \) is the earliest arrival packet in cell \( i_1 \) at time \( t - 1 \).

As we assume that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied at time \( t + j_1 - \ell_{i_1} \) (note that \( t + j_1 - \ell_{i_1} \leq t - 1 \)), we see that \( d(t + j_1 - \ell_{i_1}) = 1 \) only if \( c(t + j_1 - \ell_{i_1}) = 1 \), and hence we have

\[
d_{2k}(t + j_1 - \ell_{i_1}) = d(t + j_1 - \ell_{i_1}) \leq c(t + j_1 - \ell_{i_1}).
\] (133)

It then follows from (22), \( a_j(t') = d_{j-1}(t') \) for all \( 1 \leq j \leq 2k \) and \( t' \geq 0 \), (129), (133), \( k \leq i_1 \leq 2k \), (3), and \( j_1 \geq 1 \) that

\[
\sum_{j=i_1+1}^{2k} q_j(t + j_1 - \ell_{i_1} - 1) - c(t + j_1 - \ell_{i_1})
\]

\[
= \sum_{j=i_1+1}^{2k} \left( q_j(t - 1) - \sum_{t'=t+j_1-\ell_{i_1}}^{t-1} (a_j(t') - d_j(t')) \right) - c(t + j_1 - \ell_{i_1})
\]

\[
= \sum_{j=i_1+1}^{2k} q_j(t - 1) - \sum_{t'=t+j_1-\ell_{i_1}}^{t-1} \sum_{j=i_1+1}^{2k} (a_j(t') - d_j(t')) - c(t + j_1 - \ell_{i_1})
\]

\[
= \sum_{j=i_1+1}^{2k} q_j(t - 1) - \sum_{t'=t+j_1-\ell_{i_1}}^{t-1} \sum_{j=i_1+1}^{2k} (d_{j-1}(t') - d_j(t')) - c(t + j_1 - \ell_{i_1})
\]

\[
= \sum_{j=i_1+1}^{2k} q_j(t - 1) - \sum_{t'=t+j_1-\ell_{i_1}}^{t-1} (d_{i_1}(t') - d_{2k}(t')) - c(t + j_1 - \ell_{i_1})
\]

\[
= - \sum_{t'=t+j_1-\ell_{i_1}}^{t-1} d_{i_1}(t') + \sum_{t'=t+j_1-\ell_{i_1}+1}^{t-1} d_{2k}(t') + d_{2k}(t + j_1 - \ell_{i_1}) - c(t + j_1 - \ell_{i_1})
\]

\[
\leq \sum_{t'=t+j_1-\ell_{i_1}+1}^{t-1} d_{2k}(t') \leq \ell_{i_1} - j_1 - 1 \leq \sum_{j=i_1+1}^{2k} \ell_j - j_1 \leq \sum_{j=i_1+1}^{2k} \ell_j - 1.
\] (134)

Since packet \( p \) is stored in buffer \( b_{i_1}(\ell_{i_1} - 1) \) at time \( t + j_1 - \ell_{i_1} \), we then consider the following two possible subcases.

Subcase 3.2(a): Packet \( p \) is stored in buffer \( b_{i_1}(0) \) at time \( t + j_1 - \ell_{i_1} - 1 \) and switch \( i_1 \) is set to the “bar” state at time \( t + j_1 - \ell_{i_1} \) so that packet \( p \) is stored in buffer \( b_{i_1}(\ell_{i_1} - 1) \) at time \( t + j_1 - \ell_{i_1} \) (see Figure 28(a)). As packet \( p \) is stored in buffer \( b_{i_1}(0) \) at time \( t + j_1 - \ell_{i_1} - 1 \), we have

\[
q_{i_1}(t + j_1 - \ell_{i_1} - 1) \neq 0.
\] (135)
Since switch $i_1$ is set to the “bar” state at time $t + j_1 - \ell_{i_1}$, it is clear that packets stored in cell $i_1$ at time $t + j_1 - \ell_{i_1}$ are the exactly those stored in cell $i_1$ at time $t + j_1 - \ell_{i_1} - 1$. Since packet $p$ is the earliest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1}$, it then follows that packet $p$ is also the earliest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1} - 1$, and hence we have from the definition of $r_{i_1}(t + j_1 - \ell_{i_1})$ that $r_{i_1}(t + j_1 - \ell_{i_1}) = 0$. Therefore, we see from $k \leq i_1 < 2k$, $q_{i_1}(t + j_1 - \ell_{i_1} - 1) \neq 0$ in (135), $r_{i_1}(t + j_1 - \ell_{i_1}) = 0$, (134), and (20) that switch $i_1$ is set to the “cross” state at time $t + j_1 - \ell_{i_1}$, and this contradicts to the condition that switch $i_1$ is set to the “bar” state at time $t + j_1 - \ell_{i_1}$ in this subcase.

**Subcase 3.2(b):** Packet $p$ is routed to the input link of cell $i_1$ at time $t + j_1 - \ell_{i_1}$ and switch $i_1$ is set to the “cross” state at time $t + j_1 - \ell_{i_1}$ so that packet $p$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1)$ at time $t + j_1 - \ell_{i_1}$ (see Figure 28(b)). In this subcase, we prove by contradiction that cell $i_1$ is empty at time $t + j_1 - \ell_{i_1} - 1$, i.e.,

\[
q_{i_1}(t + j_1 - \ell_{i_1} - 1) = 0. \tag{136}
\]

Suppose that $q_{i_1}(t + j_1 - \ell_{i_1} - 1) \neq 0$. Let packet $p'$ be the latest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1} - 1$. As packet $p$ is routed to the input link of cell $i_1$ at time $t + j_1 - \ell_{i_1}$, it follows from Lemma 10 (note that $t + j_1 - \ell_{i_1} \leq t - 1$) that $p = p' + 1$, i.e., $p' = p - 1$. Thus, packet $p - 1$ is the latest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1} - 1$. From Lemma 8 (note that $t + j_1 - \ell_{i_1} \leq t - 1$), we can see that packet $p - 1$ is stored in buffer $b_{i_1}(\ell_{i_1} - 1)$ at time $t + j_1 - \ell_{i_1} - 1$. It follows that packet $p - 1$ is stored in buffer $b_{i_1}(\ell_{i_1} - 2)$ at time $t + j_1 - \ell_{i_1}$. Since we have shown that packet $p$ is the earliest arrival packet in cell $i_1$ at time $t + j_1 - \ell_{i_1}$, a contradiction is reached.

From $k \leq i_1 < 2k$, $q_{i_1}(t + j_1 - \ell_{i_1} - 1) = 0$ in (136), (134), and (19), we see that switch $i_1$ is set to the “bar” state at time $t + j_1 - \ell_{i_1}$, and this contradicts to the condition that switch $i_1$ is set to the “cross” state at time $t + j_1 - \ell_{i_1}$ in this subcase.

Now we know that packet $p$ is the earliest arrival packet in cell $i_1$ at time $t - 1$ and it is stored in buffer $b_{i_1}(0)$ at time $t - 1$. It is clear from the definition of $r_{i_1}(t)$ that $r_{i_1}(t) = 0$. From
\( k \leq i_1 < 2k, \ q_{i_1}(t-1) \neq 0 \) in (128), \( r_{i_1}(t) = 0 \), (130), and (20), we see that switch \( i_1 \) is set to the “cross” state at time \( t \). From (129), (130), and (19), we see that switch \( i \) is set to the “bar” state at time \( t \) for \( i = i_1 + 1, i_1 + 2, \ldots, 2k \). As such, packet \( p \) is routed to the departure link of the network element at time \( t \), and hence we have \( d(t) = 1 \) (see Figure 29).

Subcase 3.3: \( i_1 = 2k \). As \( i_1 = 2k \), we have from (128) that \( q_{2k}(t-1) \neq 0 \), i.e., \( q_{2k}(t-1) = 1 \) (as \( q_{2k}(t-1) \leq \ell_{2k} = 1 \)). Since it is clear that the packet stored in cell \( 2k \) at time \( t - 1 \) is the earliest arrival packet in cell \( 2k \) at time \( t - 1 \) and it is stored in buffer \( b_{2k}(0) \) at time \( t - 1 \), we see from the definition of \( r_{2k}(t) \) that \( r_{2k}(t) = 0 \). From \( q_{2k}(t-1) \neq 0 \) in (128), \( r_{2k}(t) = 0 \), (130), and (20), we see that switch \( 2k \) is set to the “cross” state at time \( t \). Thus, it is easy to see that the packet stored in cell \( 2k \) at time \( t - 1 \) is routed to the departure link of the network element at time \( t \), and hence we have \( d(t) = 1 \).

**Theorem 15** Suppose that \( \ell_{k-1}^k \in A_k \), (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Then the network element can be operated as a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \).

**Proof.** Note that we have shown in Lemma 4 that the flow conservation property in (P1) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied at all times.

Now we show by induction on time \( t \) that the ordered property in (A2), the circularly contiguous property in (A3), and the properties in (P2)–(P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied at time \( t \) for all \( t \geq 0 \). As the network element in Figure 1 is started from an empty system at time 0, the ordered property in (A2), the circularly contiguous property in (A3), and the properties in (P2)–(P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) hold vacuously at time \( t = 0 \). Assume as the induction hypothesis that the ordered property in (A2), the circularly contiguous property in (A3), and the properties in (P2)–(P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied up to time \( t - 1 \) for some \( t - 1 \geq 0 \). We then see from Lemma 11 that the maximum buffer usage property in (P3) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) is satisfied at time \( t \), from Lemma 12 that the ordered property in (A2) and the FIFO departure property in (P4) of Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) are satisfied at time \( t \), from Lemma 13 that the circularly contiguous property in (A3) is satisfied at time \( t \), and from Lemma 14 that the nonidling property in (P2) of
Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at time $t$. Therefore, the induction is completed and we have proved Theorem 15.

Remark 16 Suppose that $\ell_0^{k-1} \in A_k$, (A1) is satisfied, and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Then we have shown in Theorem 15 that the nonidling property in (P2) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ is satisfied at all times, and it follows from Lemma 11 that $q(t) \leq \sum_{j=k}^{2k} \ell_j$ for all $t \geq 0$.

Theorem 17 Suppose that $\ell_0^{k-1} \in A_k$ and the network element in Figure 1 is started from an empty system at time 0 and is operated according to the explicit control scheme in (C1)–(C3). Then the network element can be operated as a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ only if (A1) is satisfied.

Proof. We prove Theorem 17 by contradiction. In the following, we divide the proof into three parts: (i) The condition in (2) is not satisfied; (ii) The condition in (3) is not satisfied; (iii) The condition in (4) is not satisfied.

(i) The condition in (2) is not satisfied. Suppose that $\ell_k \geq \sum_{j=0}^{k-1} \ell_j + 2$. Let $x = \sum_{j=0}^{k-1} \ell_j + 1$ (note that $\ell_k - x \geq 1$). It is clear that we have $I_j(x; \ell_0^{k-1}) = 1$ for $j = 0, 1, \ldots, k - 1$ in the $C$-transform $(I_0(x; \ell_0^{k-1}), I_1(x; \ell_0^{k-1}), \ldots, I_{k-1}(x; \ell_0^{k-1}))$ of $x$ with respect to the $k$-vector $\ell_0^{k-1} = (\ell_0, \ell_1, \ldots, \ell_{k-1})$. Thus, we have

$$\sum_{j=0}^{k-1} I_j(x; \ell_0^{k-1}) \ell_j = \sum_{j=0}^{k-1} \ell_j = x - 1. \quad (137)$$

Let $t' = \sum_{j=k+1}^{2k} \ell_j + 1$. Consider the following scenario:

$$a(t) = 1, \text{ for } 1 \leq t \leq t', \quad (138)$$
$$a(t) = 0, \text{ for } t' + 1 \leq t \leq t' + \ell_k - x, \quad (139)$$
$$a(t' + \ell_k - x + 1) = 1, \quad (140)$$
$$a(t) = 0, \text{ for } t' + \ell_k - x + 2 \leq t \leq t' + \ell_k, \quad (141)$$
$$c(t) = 0, \text{ for } 1 \leq t \leq t' + \ell_k. \quad (142)$$

Since we assume that the network element in Figure 1 is operated as a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$, we see from (138) and $t' + 1 = \sum_{j=k+1}^{2k} \ell_j + 2 \leq \sum_{j=k}^{2k} \ell_j$ (note that $\ell_k \geq 2$) that arrival packets from the arrival link of the network element during the time period $[1, t']$ and the arrival packet from the arrival link of the network element at time $t' + \ell_k - x + 1$ are all admitted into the network element.

Let

$$t_i = \sum_{j=2k+1-i}^{2k} \ell_j, \text{ for } 0 \leq i \leq k. \quad (143)$$
Note from (143) that $t' = t_k + 1$. Consider some $1 \leq t \leq t'$ and let $i(t)$ be the greatest nonnegative integer such that $t_{i(t)} + 1 \leq t$, i.e.,

$$i(t) = \max\{0 \leq i \leq k : t_{i(t)} + 1 \leq t\}.$$ 

We first claim that for $1 \leq t \leq t'$, packet $p$ is stored in buffer $b_{2k-i}((p - t - 1) \mod \ell_{2k-i})$ at time $t$ for $t_i + 1 \leq p \leq t_{i+1}$ and $0 \leq i \leq i(t) - 1$ (note that we have from (143) that there are $t_{i+1} - t_i = \ell_{2k-i}$ packets in cell $2k - i$ at time $t$) and packet $p$ is stored in buffer $b_{2k-i(t)}((p - t - 1) \mod \ell_{2k-i(t)})$ at time $t$ for $t_{i(t)} + 1 \leq p \leq t$. We show the claim by induction on $1 \leq t \leq t'$.

As the network element in Figure 1 is started from an empty system at time 0, we have $q(0) = 0$. From (8), it is then clear that

$$q_i(0) = 0, \text{ for } 0 \leq i \leq 2k. \quad (144)$$

By using the same argument as in Case 2 in the proof of Lemma 14, we can show that switch $i$ is set to the “bar” state at time 1 for $i = 0, 1, \ldots, k - 1$. Furthermore, from (144) and $c(1) = 0$, we have

$$\sum_{j=i+1}^{2k} q_j(0) - c(1) = 0 < \sum_{j=i+1}^{2k} \ell_j, \text{ for } k \leq i \leq 2k - 1, \quad (145)$$

$$\sum_{j=2k+1}^{2k} q_j(0) - c(1) = 0 = \sum_{j=2k+1}^{2k} \ell_j. \quad (146)$$

Thus, we see from $q_i(0) = 0$ in (144), (145), and (19) that switch $i$ is set to the “bar” state at time 1 for $i = k, k + 1, \ldots, 2k - 1$, and we see from $q_{2k}(0) = 0$ in (144), (146), and (19) that switch $2k$ is set to the “cross” state at time 1. Therefore, the packet admitted into the network element at time 1 is routed into the fiber delay line in cell $2k$ at time 1 and is stored in buffer $b_{2k}(0)$ at time 1. Thus, the claim holds for $t = 1$.

Assume as the induction hypothesis that the claim holds for some $1 \leq t \leq t' - 1$. We then consider the two cases $t_{i(t)} + 1 \leq t < t_{i(t)+1}$ and $t = t_{i(t)+1}$ separately.

**Subcase 1.1:** $t_{i(t)} + 1 \leq t < t_{i(t)+1}$. In this case, we have from the induction hypothesis that

$$q_i(t) = 0 \text{ for } 0 \leq i \leq 2k - i(t) - 1, \text{ and } q_{2k-i(t)}(t) = t - t_{i(t)}; \quad (147)$$

$$q_i(t) = \ell_i, \text{ for } 2k - i(t) + 1 \leq i \leq 2k. \quad (148)$$

Furthermore, we also see that the earliest (resp., latest) arrival packet in cell $2k - i(t)$ at time $t$, i.e., packet $t_{i(t)} + 1$ (resp., packet $t$), is stored in buffer $b_{2k-i(t)}((t_{i(t)} + 1 - t - 1) \mod \ell_{2k-i(t)}) = b_{2k-i(t)}(\ell_{2k-i(t)} + t_{i(t)} - t)$ (resp., $b_{2k-i(t)}((t - t - 1 \mod \ell_{2k-i(t)}) = b_{2k-i(t)}(\ell_{2k-i(t)} - 1)$) at time $t$. It follows from the definition of $r_{2k-i(t)}(t+1)$ and $s_{2k-i(t)}(t+1)$ that

$$r_{2k-i(t)}(t+1) = \ell_{2k-i(t)} + t_{i(t)} - t \text{ and } s_{2k-i(t)}(t+1) = \ell_{2k-i(t)} - 1, \quad (149)$$

$$s_{2k-i(t)}(t+1) = t_{i(t)} + 1 \text{ and } q_{2k-i(t)}(t) = 0.$$
and hence we have from (9) that
\[ w_{2k-i(t)}(t+1) = 0. \] (150)

From \( r_{2k-i(t)}(t+1) = \ell_{2k-i(t)} + t_{i(t)} - t \) in (149) and \( q_{2k-i(t)}(t) = t - t_{i(t)} \) in (147), we have
\[ r_{2k-i(t)}(t+1) + q_{2k-i(t)}(t) = \ell_{2k-i(t)}. \] (151)

Note from \( 1 \leq t \leq t' - 1 \) and (143) that \( 0 \leq i(t) \leq k \). From \( 0 \leq i(t) \leq k \), we have \( 2k - i(t) \geq k \). It is then clear from (147), (148), \( 2k - i(t) \geq k \), and (8) that
\[ q^{(1)}(t) = 0 \text{ and } q^{(2)}(t) \neq 0. \] (152)

From (152), (147), and (148), we see that the cell index \( j(t+1) \) as defined in (14) is given by
\[ j(t+1) = 2k - i(t). \] (153)

From (153) and (150), we have
\[ w_{j(t+1)}(t+1) = w_{2k-i(t)}(t+1) = 0. \] (154)

From (147), (148), and \( c(t+1) = 0 \), we see that
\[ \sum_{j=i+1}^{2k} q_j(t) - c(t+1) < \sum_{j=i+1}^{2k} \ell_j, \text{ for } k \leq i \leq 2k - i(t) - 1, \] (155)
\[ \sum_{j=i+1}^{2k} q_j(t) - c(t+1) = \sum_{j=i+1}^{2k} \ell_j, \text{ for } 2k - i(t) \leq i \leq 2k, \] (156)

Furthermore, for cell \( i \) with \( r_i(t+1) \neq 0 \), where \( 2k - i(t) + 1 \leq i \leq 2k \), we see from (148) and the nonnegativity of \( r_i(t+1) \) that
\[ r_i(t+1) + q_i(t) > q_i(t) = \ell_i. \] (157)

Thus, we see from \( q^{(1)}(t) = 0 \) in (152), (154), and (15) that that switch \( i \) is set to the “bar” state at time \( t+1 \) for \( i = 0, 1, \ldots, k - 1 \), and we see from \( q_i(t) = 0 \) in (147), (155), and (19) that switch \( i \) is set to the “bar” state at time \( t+1 \) for \( i = k, k+1, \ldots, 2k - i(t) - 1 \), and we see from \( q_{2k-i(t)}(t) = t - t_{i(t)} \neq 0 \) in (147), \( r_{2k-i(t)}(t+1) = \ell_{2k-i(t)} + t_{i(t)} - t \neq 0 \) in (149), (151), and (20) that switch \( 2k - i(t) \) is set to the “cross” state at time \( t+1 \). Furthermore, we see from \( q_i(t) = \ell_i \neq 0 \) in (148), (156) (for those with \( r_i(t+1) = 0 \)) (resp., (157) (for those with \( r_i(t+1) \neq 0 \)), and (20) that switch \( i \) is set to the “bar” state at time \( t+1 \) for \( i = 2k - i(t) + 1, 2k - i(t) + 2, \ldots, 2k \).

Therefore, it is clear that packet \( p \) is stored in buffer \( b_{2k-i}((p-t-2) \mod \ell_{2k-i}) = b_{2k-i}((p-(t+1) - 1) \mod \ell_{2k-i}) \) at time \( t+1 \) for \( t_i + 1 \leq p \leq t_{i+1} \) and \( 0 \leq i \leq i(t) - 1 \) and packet \( p \) is stored in buffer \( b_{2k-i(t)}((p-t-2) \mod \ell_{2k-i(t)}) = b_{2k-i(t)}((p-(t+1) - 1) \mod \ell_{2k-i(t)}) \) at time \( t+1 \) for \( t_i(t) + 1 \leq p \leq t \). Furthermore, we can see that the packet admitted into the
network element at time $t + 1$ is routed into the fiber delay line in cell $2k - i(t)$ at time $t + 1$ and it is stored in buffer $b_{2k-i(t)}(\ell_{2k-i(t)} - 1) = b_{2k-i(t)}((t+1-(t+1)-1) \mod \ell_{2k-i(t)})$ at time $t + 1$. As such, the claim holds for $t + 1$ and the induction is completed.

*Subcase 1.2: $t = t_{i(t+1)}$. In this case, we have from the induction hypothesis that*

$$q_i(t) = 0, \text{ for } 0 \leq i \leq 2k - i(t) - 1,$$

$$q_i(t_i) = \ell_i, \text{ for } 2k - i(t) \leq i \leq 2k,$$

and we can show as in Case 1 of Part(i) in the proof of Theorem 17 that (150)–(154) still hold.

From (158), (159), and $c(t+1) = 0$, we have

$$\sum_{j=i+1}^{2k} q_j(t) - c(t + 1) < \sum_{j=i+1}^{2k} \ell_j, \text{ for } k \leq i \leq 2k - i(t) - 2,$$

$$\sum_{j=i+1}^{2k} q_j(t) - c(t + 1) = \sum_{j=i+1}^{2k} \ell_j, \text{ for } 2k - i(t) - 1 \leq i \leq 2k.$$  

Furthermore, for cell $i$ with $r_i(t + 1) \neq 0$, where $2k - i(t) \leq i \leq 2k$, we see from (159) and the nonnegativity of $r_i(t + 1)$ that

$$r_i(t + 1) + q_i(t) > q_i(t) = \ell_i.$$  

Thus, we see from $q_i^{(1)}(t) = 0$ in (152), (154), and (15) that that switch $i$ is set to the “bar” state at time $t + 1$ for $i = 0, 1, \ldots, k - 1$, and we see from $q_i(t) = 0$ in (158), (160), and (19) that switch $i$ is set to the “bar” state at time $t + 1$ for $i = k, k + 1, \ldots, 2k - i(t) - 2$, and we see from $q_{2k-i(t)-1}(t) = 0$ in (158), (161), and (19) that switch $2k - i(t) - 1$ is set to the “cross” state at time $t + 1$, and we see from $q_i(t) = \ell_i \neq 0$ in (159), (161) (for those with $r_i(t+1) = 0$) (resp., (162) (for those with $r_i(t+1) \neq 0$)), and (20) that switch $i$ is set to the “bar” state at time $t + 1$ for $i = 2k - i(t), 2k - i(t) + 1, \ldots, 2k$.

Therefore, it is clear that packet $p$ is stored in buffer $b_{2k-i}((p-t-2) \mod \ell_{2k-i}) = b_{2k-i}((p-(t+1)-1) \mod \ell_{2k-i})$ at time $t + 1$ for $t_i + 1 \leq p \leq t_{i+1}$ and $0 \leq i \leq i(t) - 1$ and packet $p$ is stored in buffer $b_{2k-i(t)}((p-t-2) \mod \ell_{2k-i(t)}) = b_{2k-i(t)}((p-(t+1)-1) \mod \ell_{2k-i(t)})$ at time $t + 1$ for $t_{i(t)+1} \leq p \leq t$. Furthermore, we can see that the packet admitted into the network element at time $t + 1$ is routed into the fiber delay line in cell $2k - i(t) - 1$ at time $t + 1$ and it is stored in buffer $b_{2k-i(t)-1}(\ell_{2k-i(t)-1} - 1)$ at time $t + 1$. Thus, the claim holds for $t + 1$ and the induction is completed.

We next claim that for $t' + 1 \leq t \leq t' + \ell_k - x$, packet $p$ is stored in buffer $b_{2k-i}((p-t-1) \mod \ell_{2k-i})$ at time $t$ for $t_i + 1 \leq p \leq t_{i+1}$ and $0 \leq i \leq k - 1$ (note that we have from (143) that there are $t_{i+1} - t_i = \ell_{2k-i}$ packets in cell $2k - i$ at time $t$) and packet $t'$ is stored in buffer $b_{k}(((t' - t - 1) \mod \ell_k)$ at time $t$. We show this claim by induction on $t' + 1 \leq t \leq t' + \ell_k - x$.

From the first claim shown above, we see that packet $p$ is stored in buffer $b_{2k-i}((p-t'-1) \mod \ell_{2k-i})$ at time $t'$ for $t_i + 1 \leq p \leq t_{i+1}$ and $0 \leq i \leq k - 1$ (note that we have from (143)
that there are \( t_{i+1} - t_i = \ell_{2k-1} \) packets in cell \( 2k - i \) at time \( t' \) and packet \( t' \) is stored in buffer \( b_k(\ell_k - 1) \) at time \( t' \). Since packet \( t' \) is stored in buffer \( b_k(\ell_k - 1) \) at time \( t' \), we can see that packet \( t' \) is stored in buffer \( b_k(\ell_{k-1} - j) \) at time \( t' + j \) for \( j = 0, 1, \ldots, \ell_k - 1 \). Note that we also have

\[
q_k(t') = 1 \text{ and } q_i(t') = \ell_i, \text{ for } k + 1 \leq i \leq 2k. \tag{163}
\]

From (163) and \( c(t' + 1) = 0 \), we have

\[
\sum_{j=i+1}^{2k} q_j(t') - c(t' + 1) = \sum_{j=i+1}^{2k} \ell_j, \text{ for } k \leq i \leq 2k. \tag{164}
\]

Furthermore, for cell \( i \) with \( r_i(t' + 1) \neq 0 \), where \( k + 1 \leq i \leq 2k \), we see from (163) and the nonnegativity of \( r_i(t' + 1) \) that

\[
r_i(t' + 1) + q_i(t') > q_i(t') = \ell_i. \tag{165}
\]

Thus, we see from \( q_i(t') = \ell_i \neq 0 \) in (163), (164) (for those with \( r_i(t' + 1) = 0 \)) (resp., (165) (for those with \( r_i(t' + 1) \neq 0 \)), and (20) that switch \( i \) is set to the “bar” state at time \( t' + 1 \) for \( i = k + 1, k + 2, \ldots, 2k \). Therefore, it is clear that packet \( p \) is stored in buffer \( b_{2k-i}((p - t' - 2) \mod \ell_{2k-i}) = b_{2k-i}((p - (t' + 1) - 1) \mod \ell_{2k-i}) \) at time \( t' + 1 \) for \( t_{i+1} \leq p \leq t_{i+1} \) and \( 0 \leq i \leq k - 1 \). As there is no packet routed into the fiber delay in cell \( k \) at time \( t' + 1 \), packet \( t' \) is still the only packet in cell \( k \) at time \( t' + 1 \) and it is stored in buffer \( b_k(\ell_k - 2) = b_k((t' - (t' + 1) - 1) \mod \ell_k) \) at time \( t' + 1 \). As such, the claim holds for \( t' + 1 \).

Assume as the induction hypothesis that this claim holds for some \( t' + 1 \leq t \leq t' + \ell_k - x - 1 \). It follows from the induction hypothesis that (163)–(165) hold with \( t' \) replaced by \( t \). Thus, we see from \( q_i(t) = \ell_i \neq 0 \) in (163), (164) (for those with \( r_i(t + 1) = 0 \)) (resp., (165) (for those with \( r_i(t + 1) \neq 0 \)), and (20) that switch \( i \) is set to the “bar” state at time \( t + 1 \) for \( i = k + 1, k + 2, \ldots, 2k \). It is then clear from the induction hypothesis that packet \( p \) is stored in buffer \( b_{2k-i}((p - t - 2) \mod \ell_{2k-i}) = b_{2k-i}((p - (t + 1) - 1) \mod \ell_{2k-i}) \) at time \( t + 1 \) for \( t_{i+1} \leq p \leq t_{i+1} \) and \( 0 \leq i \leq k - 1 \). As we have \( a(t) = 0 \) for \( t' + 1 \leq t \leq t' + \ell_k - x \) in (139), it is clear that there is no packet routed into the fiber delay in cell \( k \) at time \( t + 1 \). We then see from the induction hypothesis that packet \( t' \) is still the only packet in cell \( k \) at time \( t + 1 \) and it is stored in buffer \( b_k((t' - (t + 1) - 1) \mod \ell_k) \) at time \( t + 1 \). As such, the claim holds for \( t + 1 \) and the induction is completed.

From the second claim shown above, we see that

\[
q^{(1)}(t' + \ell_k - x) = 0 \text{ and } q^{(2)}(t' + \ell_k - x) \neq 0. \tag{166}
\]

and the cell index \( j(t' + \ell_k - x + 1) \) as defined in (14) is given by

\[
j(t' + \ell_k - x + 1) = k. \tag{167}
\]
Furthermore, as packet $t'$ is the only packet in cell $k$ at time $t' + \ell_k - x$ and it is stored in buffer $b_k(x - 1)$ at time $t' + \ell_k - x$, it follows from (9) and $0 < x - 1 = \sum_{j=0}^{k-1} \ell_j < \ell_k - 1$ that
\[ w_k(t' + \ell_k - x + 1) = x. \] (168)

From (167) and (168), we have
\[ w_j(t' + \ell_k - x + 1) = w_k(t' + \ell_k - x + 1) = x. \] (169)

From (137) and (166)–(169), we can show that packet $t' + 1$ is routed to the output link of cell $k - 1$ at time $t' + \ell_k - x + 1 + \sum_{j=0}^{k-1} l_j(x; \ell_j^{k-1}) = t' + \ell_k$ by using the same argument as in the proof of Lemma 6(ii). Since there are $t' + 1$ arrival packets during the time period $[1, t' + \ell_k]$, the first $t'$ packets is stored in the last $k + 1$ cells at time $t' + \ell_k - x$, and the arrival packet from the arrival link of the network element at time $t' + \ell_k - x + 1$ is routed to the output link of cell $k - 1$ at time $t' + \ell_k$, it follows that there is no packet routed into fiber delay line in cell $k$ during the time period $[t' + \ell_k - x + 1, t' + \ell_k - 1]$. As we have $c(t) = 0$, for $t' + \ell_k - x + 2 \leq t \leq t' + \ell_k$ in (142), we can show that packet $p$ is stored in buffer $b_{2k-i}((p - (t' + \ell_k - 1) - 1) \mod \ell_{2k-i})$ at time $t' + \ell_k - 1$ for $t_i + 1 \leq p \leq t_i+1$ and $0 \leq i \leq k - 1$ (note that we have from (143) that there are $t_{i+1} - t_i = \ell_{2k-i}$ packets in cell $2k-i$ at time $t' + \ell_k - 1$ and packet $t'$ is stored in buffer $b_k(0)$ at time $t' + \ell_k - 1$. by using the same argument as in the argument in the second claim above. Thus, we have
\[ q_k(t' + \ell_k - 1) = 1 \text{ and } q_i(t' + \ell_k - 1) = \ell_i, \text{ for } k + 1 \leq i \leq 2k, \] (170)
and we also have from the definition of $r_k(t' + \ell_k)$ that
\[ r_k(t' + \ell_k) = 0. \] (171)

From (170) and $c(t' + \ell_k) = 0$, it is clear that
\[ \sum_{j=i+1}^{2k} q_j(t' + \ell_k - 1) - c(t' + \ell_k) = \sum_{j=i+1}^{2k} \ell_j, \text{ for } k \leq i \leq 2k. \] (172)

Furthermore, for cell $i$ with $r_i(t' + \ell_k) \neq 0$, where $k + 1 \leq i \leq 2k$, we see from (170) and the nonnegativity of $r_i(t' + \ell_k)$ that
\[ r_i(t' + \ell_k) + q_i(t' + \ell_k - 1) > q_i(t' + \ell_k - 1) = \ell_i. \] (173)

Thus, we see from $q_k(t' + \ell_k - 1) \neq 0$ in (170), (171), (172), and (20) that switch $k$ is set to the “bar” state at time $t' + \ell_k$, and we see from $q_i(t' + \ell_k - 1) = \ell_i \neq 0$ in (170), (172) (for those with $r_i(t' + \ell_k) = 0$) (resp., (173) (for those with $r_i(t' + \ell_k) \neq 0$)), and (20) that switch $i$ is set to the “bar” state at time $t' + \ell_k$ for $i = k + 1, k + 2, \ldots, 2k$. As packet $t' + 1$ is routed to the output link of cell $k - 1$ at time $t' + \ell_k$, it follows that packet $t' + 1$ is routed to the departure link of the network element at time $t' + \ell_k$, contradicting to the nonidling property in (P2) of FIFO queues as we have $c(t' + \ell_k) = 0$. 

(ii) The condition in (3) is not satisfied. Since the condition in (3) is not satisfied, it can be that there are two possible cases to consider.

Case 1: $\ell_{2k} \geq 2$. Consider the following scenario: $a(1) = 1$, $c(1) = 0$, and $c(2) = 1$. As $q(0) - c(1) = 0 < \sum \ell_j$, we have from (12) that $a_0(1) = a(1) = 1$, i.e., the arrival packet from the arrival link of the network element at time 1 is admitted into the network element at time 1.

Note that we can show that (144)–(146) still hold. Thus, we see from $a_i(0) = 0$ in (144), (145), and (19) that switch $i$ is set to the “bar” state at time 1 for $i = k, k + 1, \ldots, 2k - 1$, and we see from $q_{2k}(0) = 0$ in (144), (146), and (19) that switch $2k$ is set to the “cross” state at time 1. Therefore, packet 1 is routed into the fiber delay line in cell $2k$ at time 1. As $\ell_{2k} \geq 2$, it requires at least 2 time slots for packet 1 to traverse through the fiber delay line in cell $2k$, and hence it is clear that packet 1 cannot be routed to the departure link of the network element in Figure 1 at time 2. However, as we assume that the network element in Figure 1 is operated as a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$, we have from (12) that $a(1) = 1$, $c(1) = 0$, $c(2) = 1$, the nonidling property in (P2), and the FIFO departure property in (P4) that packet 1 should be routed to the departure link of the network element at time 2. As such, we have reached a contradiction.

Case 2: $\ell_i \geq \sum_{j=i+1}^{2k} \ell_j + 2$, for some $k \leq i_1 \leq 2k - 1$. Let $t' = \sum_{j=i_1+1}^{2k} \ell_j + 1$. Consider the following scenario:

\begin{align*}
  a(t) &= 1 \quad \text{and} \quad c(t) = 0 \quad \text{for} \quad 1 \leq t \leq t', \quad (174) \\
  c(t) &= 1, \quad \text{for} \quad t' + 1 \leq t \leq 2t'. \quad (175)
\end{align*}

By using the same argument as in the first claim of Part(i) in the proof of Theorem 17, we can show that packet $t'$ is stored in buffer $b_{i_1}((t' - t' - 1) \mod \ell_i) = b_{i_1}(\ell_i - 1)$ at time $t'$. As $\ell_i \geq \sum_{j=i_1+1}^{2k} \ell_j + 2 = t' + 1$, it requires at least $t' + 1$ time slots for packet $t'$ to traverse through the fiber delay line in cell $i_1$, and hence it is clear that packet $t'$ cannot be routed to the departure link of the network element in Figure 1 before time $2t' + 1$. However, as we assume that the network element in Figure 1 is operated as a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$, and hence we have from (174), (175), the nonidling property in (P2), and the FIFO departure in (P4) that packet $t'$ should be routed to the departure link of the network element at time $2t'$. As such, we have reached a contradiction.

(iii) The condition in (4) is not satisfied. Suppose that

\begin{align*}
  u &= (\ell_i \mod \ell_{i+1}) \neq 0, \quad \text{for} \quad k \leq i_1 \leq 2k - 1, \quad (176) \\
  \ell_i \mod \ell_{i+1} &= 0, \quad \text{for} \quad i_1 + 1 \leq i \leq 2k - 1. \quad (177)
\end{align*}

It is clear from (176) that

\begin{align*}
  (\ell_{i_1} - u) \mod \ell_{i_1+1} &= 0. \quad (178)
\end{align*}
Let \( t' = \sum_{j=i_1+1}^{2k} \ell_j + \ell_{i_1} - u \). Consider the following scenario:

\[
a(t) = 1 \text{ and } c(t) = 0, \text{ for } 1 \leq t \leq t', \tag{179}
\]

\[
c(t' + 1) = 1 \text{ and } c(t) = 0, \text{ for } t' + 2 \leq t \leq t' + u + 1. \tag{180}
\]

Let

\[
t_i = \sum_{j=2k+1-i}^{2k} \ell_j, \text{ for } 0 \leq i \leq 2k - i_1. \tag{181}
\]

Note from (181) that \( t' = t_{2k-i_1} + (\ell_{i_1} - u) \). By using the same argument as in the first claim of Part(i) in the proof of Theorem 17, we can show that packet \( p \) is stored in buffer \( b_{2k-i_1}((p-t'-1) \mod \ell_{2k-i_1}) \) at time \( t' \) for \( t_i + 1 \leq p \leq t_{i+1} \) and \( 0 \leq i \leq 2k - i_1 - 1 \) (note that we have from (181) that there are \( t_{i+1} - t_i = \ell_{2k-i} \) packets in cell \( 2k - i \) at time \( t' \) and packet \( p \) is stored in buffer \( b_{i_1}((p-t'-1) \mod \ell_{i_1}) \) at time \( t' \) for \( t_{2k-i_1} + 1 \leq p \leq t' \) (note that we have from (181) that there are \( t' - t_{2k-i_1} = \ell_{i_1} - u \) packets in cell \( i_1 \) at time \( t' \)). Thus, we have

\[
q_i(t') = 0, \text{ for } 0 \leq i \leq i_1 - 1 \text{ and } q_{i_1}(t') = \ell_{i_1} - u \neq 0, \tag{182}
\]

\[
q_i(t') = \ell_i, \text{ for } i_1 + 1 \leq i \leq 2k. \tag{183}
\]

As packet \( p \) is stored in buffer \( b_{i_1}((p-t'-1) \mod \ell_{i_1}) = b_{i_1}(\ell_{i_1} + p - t' - 1) \) at time \( t' \) for \( t_{2k-i_1} + 1 \leq p \leq t' \), we see that packet \( p \) is stored in buffer \( b_{i_1}(\ell_{i_1} + p - t' - 1 - j) \) at time \( t' + j \) for \( t_{2k-i_1} + 1 \leq p \leq t' \) and \( 1 \leq j \leq u \). From \( u \neq 0 \), we see that buffer \( b_{i_1}(0) \) is empty at time \( t' \). Since the earliest arrival packet in cell \( i_1 \) at time \( t' \), i.e., packet \( t_{2k-i_1} + 1 \), is stored in buffer \( b_{i_1}(u) \) at time \( t' \), it then follows from the definition of \( r_{i_1}(t'+1) \) that

\[
r_{i_1}(t'+1) = u \neq 0. \tag{184}
\]

From (182) and (184), we have

\[
r_{i_1}(t'+1) + q_{i_1}(t') = \ell_{i_1}. \tag{185}
\]

Furthermore, it is also clear that packet \( t_{2k-i_1} + 1 \) remains the earliest arrival packet in cell \( i_1 \) at time \( t' + j \) and is stored in buffer \( b_{i_1}(u - j) \) at time \( t' + j \) for \( 1 \leq j \leq u \).

We also note that the earliest arrival packet in cell \( 2k - i \) at time \( t' \), i.e., packet \( t_i + 1 \), is stored in buffer \( b_{2k-i}((t_i - t') \mod \ell_{2k-i}) \) at time \( t' \) for \( i = 0, 1, \ldots, 2k - i_1 - 1 \). From the definition of \( r_i(t'+1) \), \( t' - t_i = (\ell_{i_1} - u) + \sum_{j=i_1+1}^{2k-i} \ell_j \), (177), and (178), we have

\[
r_{2k-i}(t'+1) = (t_i - t') \mod \ell_{2k-i}
= \left[ -(\ell_{i_1} - u) - \sum_{j=i_1+1}^{2k-i} \ell_j \right] \mod \ell_{2k-i} = 0, \text{ for } 0 \leq i \leq 2k - i_1 - 1. \tag{186}
\]
From (183) and \( c(t'+1) = 1 \), we have

\[
\sum_{j=i+1}^{2k} q_j(t') - c(t'+1) < \sum_{j=i+1}^{2k} \ell_j, \quad \text{for } i_1 + 1 \leq i \leq 2k. \tag{187}
\]

We see from \( q_{i_1}(t') = \ell_{i_1} - u \neq 0 \) in (182), \( r_{i_1}(t'+1) \neq 0 \) in (184), (185), and (20) that switch \( i_1 \) is set to the “cross” state at time \( t'+1 \), and we see from \( q_i(t') = \ell_i \neq 0 \) in (183), \( r_i(t'+1) = 0 \) in (186), (187), and (20) that switch \( i \) is set to the “cross” state at time \( t'+1 \) for \( i = i_1 + 1, i_1 + 2, \ldots, 2k \).

Therefore, we can see that packet \( p+1 \) is stored in buffer \( b_{2k-i}((p-t'-1) \mod \ell_{2k-i}) \) at time \( t'+1 \) for \( t_i + 1 \leq p \leq t_{i+1} \) and \( 0 \leq i \leq 2k - i_1 - 2 \), and packet \( p \) is stored in buffer \( b_{i+1}((p-t'-2) \mod \ell_{i+1}) \) at time \( t'+1 \) for \( t_{2k-i_1-1} + 2 \leq p \leq t_{2k-i} \). Moreover, since buffer \( b_{i_1}(0) \) is empty at time \( t' \), it follows that there is no packet routed into the fiber delay line in cell \( i_1 + 1 \) at time \( t'+1 \), implying that buffer \( b_{i_1+1}(0) \) is empty at time \( t'+1 \). Hence, we see that there are \( t_{2k-i_1} - t_{2k-i_1-1} - 1 = \ell_{i_1+1} - 1 \) packets in cell \( i_1 + 1 \) at time \( t'+1 \) and the earliest arrival packet in cell \( i_1 + 1 \) at time \( t'+1 \), i.e., packet \( t_{2k-i_1-1} + 2 \), is stored in buffer \( b_{i_1+1}(0) \) at time \( t'+1 \), which implies that \( r_{i_1+1}(t'+2) = 0 \).

**Case 1:** \( u = 1 \). From the above argument, we have

\[
q_{i_1+1}(t'+1) = \ell_{i_1+1} - 1 \quad \text{and} \quad r_{i_1+1}(t'+2) = 0, \tag{188}
\]

\[
q_i(t'+1) = \ell_i \quad \text{and} \quad r_i(t'+2) = 0, \quad \text{for } i_1 + 2 \leq i \leq 2k. \tag{189}
\]

From (188), (189), and \( c(t'+2) = 0 \) in (180), it follows that

\[
\sum_{j=i+1}^{2k} q_j(t'+1) - (t'+2) = \sum_{j=i+1}^{2k} \ell_j - 1 < \sum_{j=i+1}^{2k} \ell_j, \tag{190}
\]

\[
\sum_{j=i+1}^{2k} q_j(t'+1) - c(t'+2) = \sum_{j=i+1}^{2k} \ell_j, \quad \text{for } i_1 + 1 \leq i \leq 2k. \tag{191}
\]

Furthermore, for cell \( i \) with \( r_i(t'+2) \neq 0 \), where \( i_1 + 2 \leq i \leq 2k \), we see from \( q_i(t'+1) = \ell_i \) in (189) and the nonnegativity of \( r_i(t'+2) \) that

\[
r_i(t'+2) + q_i(t'+1) > q_i(t'+1) = \ell_i. \tag{192}
\]

As the earliest packet in cell \( i_1 \) at time \( t'+1 \), packet \( t_{2k-i_1} + 1 \), is stored in buffer \( b_{i_1}(u-1) = b_{i_1}(0) \) at time \( t'+1 \), we have from the definition of \( r_{i_1}(t'+2) \) that

\[
r_{i_1}(t'+2) = 0. \tag{193}
\]

Thus, we see from \( q_{i_1}(t'+1) \neq 0 \), (193), (190), and (20) that switch \( i_1 \) is set to the “cross” state at time \( t'+2 \), and we see from \( q_{i_1+1}(t'+1) = \ell_{i_1+1} - 1 \neq 0 \) and \( r_{i_1+1}(t'+2) = 0 \) in (188), (191), and (20) that switch \( i_1 + 1 \) is set to the “bar” state at time \( t'+2 \), and we see
from \( q_i(t' + 1) = \ell_i \neq 0 \) and \( r_i(t' + 2) = 0 \) in (189), (191), and (20) that switch \( i \) is set to the “bar” state at time \( t' + 2 \) for \( i = i_1 + 2, i_1 + 3, \ldots, 2k \). Since packet \( t_{2k-i_1+1} \) is stored in buffer \( b_{i_1}(0) \) at time \( t' + 1 \), it follows that packet \( t_{2k-i_1+1} \) is routed to the departure link of the network element at time \( t' + 2 \). However, this contradicts to the nonidling property in (P2) of FIFO queues since we have \( c(t' + u + 1) = c(t' + 2) = 0 \) in (180).

**Case 2:** \( u \neq 1 \). In this case, we claim that for \( 1 \leq j \leq u \),

\[
q_{i_1+1}(t' + j) = \ell_{i_1+1} - 1 \quad \text{and} \quad r_{i_1+1}(t' + j + 1) = ((1 - j) \mod \ell_{i_1+1}), \tag{194}
\]

\[
q_i(t' + j) = \ell_i, \quad \text{for} \quad i_1 + 2 \leq i \leq 2k. \tag{195}
\]

We show the claim by induction on \( 1 \leq j \leq u \). From the paragraph above Case 1 of Part(v) in the proof of Theorem 17, it is clear that the claim holds for \( j = 1 \). Assume as the induction hypothesis that the claim holds for some \( 1 \leq j \leq u - 1 \), i.e., (194) and (195) hold for some \( 1 \leq j \leq u - 1 \). We then consider the two cases \( j = 1 \) and \( 1 < j \leq u - 1 \) separately.

**Subcase 2(a):** \( j = 1 \). In this subcase, we immediately have from the induction hypothesis that

\[
r_{i_1+1}(t' + 1 + j) = 0. \tag{196}
\]

From \( 1 \leq j \leq u - 1 \) and (180), we have \( c(t' + j + 1) = 0 \). From the induction hypothesis and \( c(t' + j + 1) = 0 \), we see that

\[
\sum_{i = i' + 1}^{2k} q_i(t' + j) - c(t' + j + 1) = \sum_{i = i' + 1}^{2k} \ell_i, \quad \text{for} \quad i_1 + 1 \leq i' \leq 2k. \tag{197}
\]

Furthermore, for cell \( i \) with \( r_i(t' + j + 1) \neq 0 \), where \( i_1 + 2 \leq i \leq 2k \), we see from \( q_i(t' + j) = \ell_i \) in (195) and the nonnegativity of \( r_i(t' + j + 1) \) that

\[
r_i(t' + j + 1) + q_i(t' + j) > q_i(t' + j) = \ell_i. \tag{198}
\]

Thus, we see from \( q_{i_1+1}(t' + j) = \ell_{i_1+1} - 1 \neq 0 \) in (194), (196), (197), and (20) that switch \( i_1 + 1 \) is set to the “bar” state at time \( t' + j + 1 \), and we see from \( q_i(t' + j) = \ell_i \neq 0 \) in (195), (197) (for those with \( r_i(t' + j + 1) = 0 \)) (resp., (198) (for those with \( r_i(t' + j + 1) \neq 0 \)), and (20) that switch \( i \) is set to the “bar” state at time \( t' + j + 1 \) for \( i = i_1 + 2, i_1 + 3, \ldots, 2k \).

Therefore, we have \( q_{i_1+1}(t' + j + 1) = q_{i_1+1}(t' + j) = \ell_{i_1+1} - 1 \) and \( q_i(t' + j + 1) = q_i(t' + j) = \ell_i \) for \( i_1 + 2 \leq i \leq 2k \). Since the earliest arrival packet in cell \( i_1 + 1 \) at time \( t' + j \) is stored in buffer \( b_{i_1+1}(0) \) at time \( t' + j \) and switch \( i_1 + 1 \) is set to the “bar” state at time \( t' + j + 1 \), we see that the earliest arrival packet in cell \( i_1 + 1 \) at time \( t' + j \) remains the earliest arrival packet in cell \( i_1 + 1 \) at time \( t' + j + 1 \) and is stored in buffer \( b_{i_1+1}(\ell_{i_1+1} - 1) \) at time \( t' + j + 1 \), which implies that \( r_{i_1+1}(t' + j + 2) = \ell_{i_1+1} - 1 \). Thus, the claim holds for \( j + 1 \) and the induction is completed.

**Subcase 2(b):** \( 1 < j \leq u - 1 \). In this subcase, we have from \( 1 < j \leq u - 1 \) and \( 0 < u \leq \ell_{i_1+1} - 1 \) that

\[
1 - \ell_{i_1+1} \leq 1 - j < 0. \tag{199}
\]
Furthermore, for cell $i$, it follows that
\[ r_{i+1}(t' + j + 1) = \ell_{i+1} - j + 1. \] (200)

From (200) and (194), we then have
\[ r_{i+1}(t' + j + 1) + q_{i+1}(t' + j) = (\ell_{i+1} - j + 1) + \ell_{i+1} - 1 = 2\ell_{i+1} - j > \ell_{i+1}. \] (201)

Thus, we see from $q_{i+1}(t' + j) = \ell_{i+1} - 1 \neq 0$, $r_{i+1}(t' + j + 1) = \ell_{i+1} - j + 1 \neq 0$ in (200), (201), and (20) that switch $i + 1$ is set to the “bar” state at time $t' + j' + 1$. Furthermore, by using the same argument as in Case 2 of Part(iv) in the proof of Theorem 17, it is clear that (197) and (198) still hold, and hence we can show that switch $i$ is set to the “bar” state at time $t' + j + 1$ for $i = i_1 + 2, i_1 + 3, \ldots, 2k$.

Therefore, we have $q_{i+1}(t' + j + 1) = q_{i+1}(t' + j) = \ell_{i+1} - 1$ and $q_i(t' + j + 1) = q_i(t' + j) = \ell_i$ for $i_1 + 2 \leq i \leq 2k$. Since the earliest arrival packet in cell $i_1 + 1$ at time $t' + j$ is stored in buffer $b_{i_1+1}(\ell_{i_1+1} - j + 1)$ at time $t' + j$ and switch $i_1 + 1$ is set to the “bar” state at time $t' + j + 1$, it is clear that the earliest arrival packet in cell $i_1 + 1$ at time $t' + j$ remains the earliest arrival packet in cell $i_1 + 1$ at time $t' + j + 1$ and is stored in buffer $b_{i_1+1}(\ell_{i_1+1} - j)$ at time $t' + j + 1$, which implies that $r_{i_1+1}(t' + j + 2) = \ell_{i_1+1} - j = ((1 - (j + 1)) \mod \ell_{i_1+1})$ in this subcase. Thus, the claim holds for $j + 1$ and the induction is completed.

From the claim shown above, we have
\[ q_{i+1}(t' + u) = \ell_{i+1} - 1 \text{ and } r_{i+1}(t' + u + 1) = \ell_{i+1} - u + 1, \] (202)
\[ q_i(t' + u) = \ell_i, \text{ for } i_1 + 2 \leq i \leq 2k. \] (203)

It is clear from (202) that
\[ r_{i_1+1}(t' + u + 1) + q_{i+1}(t' + u) = 2\ell_{i+1} - u > \ell_{i+1}. \] (204)

From (202), (203), and $c(t' + u + 1) = 0$, we have
\[ \sum_{i=i_1+1}^{2k} q_i(t' + u) - c(t' + u + 1) = \sum_{i=i_1+1}^{2k} \ell_i - 1 < \sum_{i=i_1+1}^{2k} \ell_i, \] (205)
\[ \sum_{i=i'+1}^{2k} q_i(t' + u) - c(t' + u + 1) = \sum_{i=i'+1}^{2k} \ell_i, \text{ for } i_1 + 1 \leq i' \leq 2k. \] (206)

Furthermore, for cell $i$ with $r_i(t' + u + 1) \neq 0$, where $i_1 + 2 \leq i \leq 2k$, we see from $q_i(t' + u) = \ell_i$ in (203) and the nonnegativity of $r_i(t' + u + 1)$ that
\[ r_i(t' + u + 1) + q_i(t' + u) > q_i(t' + u) = \ell_i. \] (208)
As packet $t_{2k-i}+1$ is stored in buffer $b_i(0)$ at time $t'+u$ and it is the earliest packet in cell $i_1$ at time $t'+u$, it follows from the definition of $r_{i_1}(t'+u+1)$ that
\[ r_{i_1}(t'+u+1) = 0. \] (209)
Thus, we see from $q_{i_1}(t'+u) \neq 0$, (209), (205), and (20) that switch $i_1$ is set to the “cross” state at time $t'+u+1$, and we see from $q_{j+1}(t'+u) = \ell_i - 1 \neq 0$ and $r_{j+1}(t'+u+1) = \ell_{j+1} - u + 1 \neq 0$ in (202), (204), and (20) that switch $i+1$ is set to the “bar” state at time $t'+u+1$, and we see from $q_i(t'+u) = \ell_i \neq 0$ in (203), (206) (for those with $r_i(t'+u+1) = 0$) (resp., (208) (for those with $r_i(t'+u+1) = 0$)), and (20) that switch $i$ is set to the “bar” state at time $t'+u+1$ for $i = i_1 + 2, i_1 + 3, \ldots, 2k$. Therefore, packet $t_{2k-i_1}+1$ is routed to the departure link of the network element at time $t'+u+1$, which clearly contradicts to the nonidling property in (P2) of FIFO queues as we have $c(t'+u+1) = 0$ in (177).

Although there are $\sum_{j=0}^{2k} \ell_j$ available buffers in the $2k+1$ cells in Figure 1, it is not possible to admit more than $\sum_{j=k}^{2k} \ell_j$ packets into the network element without violating the properties in (P1)–(P4) of Definition 1 for a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j$ under the explicit control scheme in (C1)–(C3). This can be shown by contradiction. Suppose that (A1) is satisfied and the network element in Figure 1 can be operated as a FIFO queue with buffer $\sum_{j=k}^{2k} \ell_j + 1$ under our explicit control scheme in (C1)–(C3).

Let
\[ t' = \sum_{j=k}^{2k} \ell_j + 1. \] (210)
Consider the scenario that $a(t) = 1$ and $c(t) = 0$ for $t = 1, 2, \ldots, t'$. Let
\[ t_i = \sum_{j=2k+1-i}^{2k} \ell_j, \text{ for } 0 \leq i \leq k+1. \] (211)
By using the same argument as in the first claim of Part(i) in the proof of Theorem 17, we can show that packet $p$ is stored in buffer $b_{2k-i}((p - (t'-1) - 1) \mod \ell_{2k-i})$ at time $t'-1$ for $t_i + 1 \leq p \leq t_i+1$ and $0 \leq i \leq k$ (note that we have from (211) that there are $t_{i+1} - t_i = \ell_{2k-i}$ packets in cell $2k-i$ at time $t'-1$). Thus, we have
\[ q_i(t'-1) = 0, \text{ for } 0 \leq i \leq k-1, \] (212)
\[ q_i(t'-1) = \ell_i, \text{ for } k+1 \leq i \leq 2k. \] (213)

Since the earliest arrival packet in cell $2k-i$ at time $t'-1$, i.e., packet $t_i + 1$, is stored in buffer $b_{2k-i}((t_i + 1 - (t'-1) - 1) \mod \ell_{2k-i})$ for $i = 0, 1, \ldots, k$, we have from the definition of $r_{2k-i}(t')$, (210), (211), and (4) that
\[ r_{2k-i}(t') = (t_i - t' + 1) \mod \ell_{2k-i} \]
\[ = \left( - \sum_{j=k}^{2k-i} \ell_j \right) \mod \ell_{2k-i} = 0, \text{ for } 0 \leq i \leq k. \] (214)
Moreover, as the latest arrival packet in cell \( k \) at time \( t' - 1 \), i.e., packet \( t' - 1 \), is stored in buffer \( b_k(t' - 1 - (t' - 1) - 1) \mod \ell_k = b_k(\ell_k - 1) \) at time \( t' - 1 \), we see from (9) that

\[
w_k(t') = 0
\]  

(215)

From (212), (213), and (8), it is clear that

\[
q^{(1)}(t' - 1) = 0 \text{ and } q^{(2)}(t' - 1) = t' - 1 \neq 0.
\]  

(216)

Furthermore, it is clear from (216), (212), and (213) that the cell index \( j(t') \) as defined in (14) is given by

\[
j(t') = k.
\]  

(217)

From (217) and (215), we have

\[
w_{j(t')}(t') = w_k(t') = 0.
\]  

(218)

Furthermore, from (213) and \( c(t') = 0 \), we can also see that

\[
\sum_{j=i+1}^{2k} q_j(t' - 1) - c(t') = \sum_{j=i+1}^{2k} \ell_j, \text{ for } k \leq i \leq 2k.
\]  

(219)

Thus, we see from \( q^{(1)}(t' - 1) = 0 \) in (216), (218), and (15) that switch \( i \) is set to the “bar” state at time \( t' \) for \( i = 0, 1, \ldots, k - 1 \), and we see from \( q_i(t' - 1) = \ell_i \neq 0 \) in (213), \( r_i(t') = 0 \) in (214), and (219) that switch \( i \) is set to the “bar” state at time \( t' \) for \( i = k, k + 1, \ldots, 2k \).

From (216) and (8), it follows that \( q(t' - 1) = q^{(1)}(t' - 1) + q^{(2)}(t' - 1) = t' - 1 \). As we assume that the network element in Figure 1 is operated as a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j + 1 \), we see from \( q(t' - 1) = t' - 1 = \sum_{j=k}^{2k} \ell_j, c(t') = 0 \), and (12) that \( a_0(t') = a(t') = 1 \), i.e., the arrival packet from the arrival link of the network element at time \( t' \) is admitted into the network element at time \( t' \). Therefore, the arrival packet from the arrival link of the network element at time \( t' \) is routed to the departure link of the network element at time \( t' \), which clearly contradicts to the nonidling property in (P2) of FIFO queues as we have \( c(t') = 0 \).

IV. Conclusion

In this paper, we considered the network element in Figure 1 and provided a simple control scheme that explicitly specifies the connection patterns of the \( 1 \times 2 \) optical crossbar switch and the \( 2k + 1 \ 2 \times 2 \) optical crossbar switches, and showed that given \( \ell_0^{k-1} = (\ell_0, \ell_1, \ldots, \ell_{k-1}) \in A_k \), the condition in (A1) is a necessary and sufficient condition on the lengths \( \ell_k, \ell_{k+1}, \ldots, \ell_{2k} \) for such a network element to be operated as an optical FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \) under our proposed control scheme.

The key idea in our explicit control scheme is to operate the network element such that packets stored in the network element satisfy the ordered property in (A2) and the circularly contiguous property in (A3), and then use these properties to show the four properties in (P1)–(P4) in Definition 1 for a FIFO queue with buffer \( \sum_{j=k}^{2k} \ell_j \).
REFERENCES


