An Embedded, Analogue Nonvolatile Memory with a Feedback-Controlled Programming Circuit On-chip

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An Embedded, Analogue Nonvolatile Memory with a Feedback-Controlled Programming Circuit On-chip

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This paper presents an analogue nonvolatile memory which is not only CMOS-compatible but also capable of storing analogue currents with a resolution of more than eight bits. The programming process is controlled by a hysteretic comparator on-chip, which stops the injection current automatically by negative feedback, regardless of the programming nonlinearity and device mismatches. With the simple, on-chip programming circuit, the proposed analogue memory is capable of storing currents ranging from 1μA to 18μA accurately with negligible variations across different memory cells.

Introduction: The neuromorphic system in [1] first employed floating-gate devices to store analogue values non-volatilely, facilitating analogue computation in parallel and in large scale. An analogue nonvolatile memory array for storing audio data was further demonstrated in [2]. While the two pioneering works were based on the customised EEPROM technology, Diorio et al. proposed the CMOS-compatible (or called *embedded*), analogue nonvolatile memory, extending its application to a wide variety of analogue circuits [3]. However, the accuracy of analogue storage in an array had been limited by the nonlinearity of programming mechanisms and device mismatches. One proposed solution was calculating the required drain

voltage for a target current, and then programming each memory cell iteratively by short pulses of injection currents [4]. This solution not only required a large, off-chip system to implement the programming algorithm but also relied on precise sensing of the drain current of each memory cell.

This paper presents an embedded, analogue nonvolatile memory, fabricated with the standard CMOS 0.35μm technology by the Taiwan Semiconductor Manufacturing Company. With a simple, on-chip programming circuit controlling the programming current by negative feedback, the memory cell is able to store analogue currents with comparable accuracy to [4]. The feedback control further eliminates the effect of device mismatches, guaranteeing a negligible variation across different memory cells.

Gate Current Models: The proposed analogue memory is based on the p-type transistor whose gate is isolated and connected with a poly-Nwell capacitor (C_{tun}), as illustrated by the inset in Fig.1. The device structure is analogous to that in [3], while a control gate formed by a second poly layer is not included and the transistor operates in the strong-inversion region instead. In each programming process, electrons in the floating gate are first removed (erased) by Fowler-Nordheim (FN) tunneling through C_{tun}. Hot-electron injection (I_{inj}) is then induced in the p-type transistor to program the floating gate. The white squares in Fig.1 show the measured I_{inj} versus the gate voltage (V_{fg}), averaged over the measurements of five transistors with W/L = 5μm/1μm. As V_{fg} increases from 1V to 6V, I_{inj} is dominated by hole and electron injections in turn, resulting in a self-convergent point around V_{fg} = 2.8V. I_{inj} preceding the self-convergent point involves both channel hot-hole injection (CHHI) and

impact-ionised hot-hole injection (IHHI), while beyond this point, only impact-ionised hot-electron injection (IHEI) is involved [5]. According to [6], CHHI in strong inversion can be modelled as Eq.(1), while IHHI and IHEI as Eq.(2).

$$I_{CHHI} = \alpha_1 I_S (|V_{DS}| - V_{DSAT})^2 e^{\frac{\beta_1}{|V_{DS}| - V_{DSAT}}} \quad (1)$$

$$I_{IHHI\&IHEI} = \alpha_2 I_S (|V_{DS}| - V_{DSAT})^3 e^{\frac{\beta_2}{|V_{DS}| - V_{DSAT}}} \quad (2)$$

where I_S represents the channel current, V_{DS} the drain-to-source voltage, and V_{DSAT} the saturation voltage. The process-dependent parameters α_i and β_i are extracted as $\alpha_1 = 6.37\times10^{-12}$ and $\beta_1 = 3.6185$ for CHHI, $\alpha_2 = 7.95\times10^{-13}$ and $\beta_2 = 6.5716$ for IHHI, and $\alpha_2 = 0.93$ and $\beta_2 = -97.427$ for IHEI. Assuming that CHHI and IHHI occur with equal probability, the total injection current is modelled as $I_{inj} = I_{IHEI} - (I_{CHHI} + I_{IHHI}) / 2$. The black curve in Fig.1 shows the simulated I_{inj}, agreeing with the measurement satisfactorily.

Proposed Circuit: Fig.2 shows the proposed analogue memory circuit and its photo. The four transistors encircled by the dotted line constitute a memory cell, wherein the common gate of M_{fg1} and M_{fg2} is the floating node (V_{fg}). M_{fg1} is the *programming transistor*, generating hot-electron injection into V_{fg} when M_{inj} turns on. C_C is added to reduce the charge-injection errors induced by the switching of M_{inj}. M_{fg2} is the *readout transistor* whose current represents the memorised current and is buffered by M_1. Compared to the single-transistor cell employed in [3], the proposed architecture has the advantage of avoiding charge injection or hot-carrier injection into V_{fg} during the readout process, as the programming current can be completely switched off by turning off M_{inj} and the drain voltage of M_{fg2} is fixed by V_{bias} through M_1. In addition, the

memorised current is independent of the characteristics of M_{fg1}, which could change or degrade after undergoing injection current for a long term. All the other transistors except for M_{10} and M_{11} form a current comparator to be shared among different memory cells. M_6-M_9 copy I_{ref} for comparison with the I_{out} copied by M_1-M_5. Through the two-stage inverter (M_{i1}-M_{i4}), the comparator controls the turning on of M_{inj} and thus the occurrence of hot-electron injection at M_{fg1}. To improve the comparator precision, M_{h1}-M_{h2} are added to introduce the hysteretic effect with its width controlled by V_{hys}. The programming procedures are as follows: (1) A voltage pulse of 8V is applied to V_{tun} to remove electrons from the floating node, causing I_{out} to be much smaller than 1μA. (2) I_{ref} ranging from 1μA to 18μA is presented. As $I_{ref} > I_{out}$, the current comparator turns on M_{inj}, inducing hot-electron injection to increase I_{out}. (3) Once I_{out} equals I_{ref}, the comparator turns off M_{inj} and stops the electron injection. The feedback control gives the great advantage of programming I_{out} automatically and accurately, regardless of the programming nonlinearity, mismatches across different memory cells, and the potential degradation of M_{fg1}. In the prototype design, a voltage buffer is also added to monitor the voltage change at V_{fg}.

Measurement Results: The inset of Fig.3 showed the measured dynamics of V_{fg} as the analogue memory was programmed to different current levels. In each experiment, V_{fg} was initialised to around 4.3V by FN tunneling, and then programmed at t = 0s when I_{ref} was presented. As I_{out} equals I_{ref}, V_{fg} converged into an equilibrium level and stored the target current reliably. The maximum programming time was around 38.3ms for I_{ref} = 18μA, shorter than

that (350ms) achieved in [4]. After I_{ref} was removed, I_{out} was measured by a source-meter (Keithley 2602). Within the range of I_{ref} = [1μA, 18μA], the maximum programming errors, $\Delta I_{out}=I_{out} - I_{ref}$, was 50nA, as depicted in Fig.3. The effective bit resolution was thus calculated as $\log_2(17/0.05)$, yielding a resolution of more than eight bits. Fig.4 plots the statistics of the measurements over four identical memory cells, revealing clearly the linearity and the precision of the analogue memory. The magnified window shows that the maximum standard deviation of 5.5nA occurs at I_{ref} = 6μA. Such a small variation is attributed to the feedback control by the comparator, and is of particular importance for an analogue memory array.

Conclusion: An embedded, analogue nonvolatile memory with a simple, on-chip programming circuit has been designed and tested. The measurement results demonstrate that the programming circuit is capable of storing analogue currents into the memory as accurately as the off-chip system in [4], with a shorter programming time and negligible variations across different memory cells. The promising performance mainly comes from the use of a hysteretic comparator to control the programming current automatically by negative feedback. To extend the application of the proposed circuit, a large array of analogue nonvolatile memory will be further developed.

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Figure captions:

Fig. 1 The measurement and simulation results of the injection current *v.s.* floating gate voltage with V_S = 6V and V_D = 0V.

Fig. 2 The full circuit of the analogue nonvolatile memory and its chip photo.

Fig. 3 The measured dynamics of V_{fg} (the inset) and the precision of the proposed analogue memory with its on-chip programming circuit.

Fig. 4 The statistics over the measurement of four analogue memory cells programmed by the on-chip, hysteretic comparator. The error bars indicate the standard deviations.

Figure 1

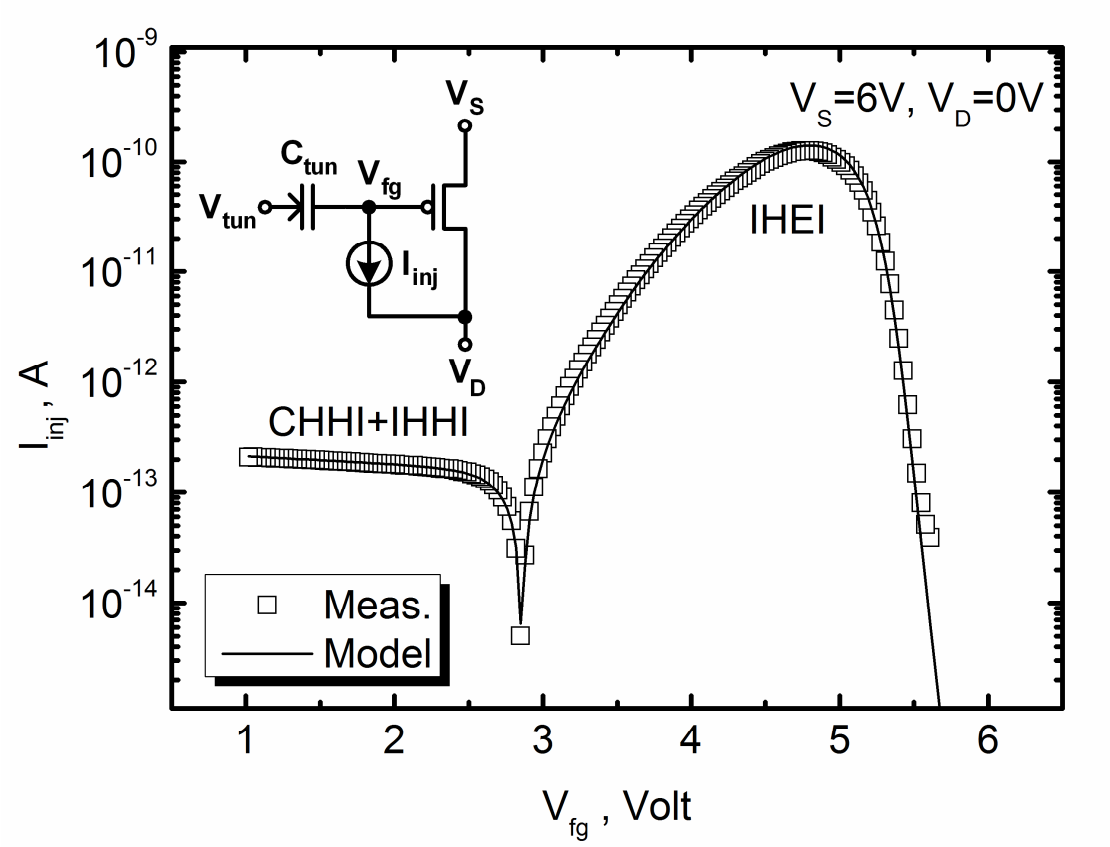
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
I_{inj}, A
1
2
3
4
5
6
V_{fg} , Volt
V_S
C_{tun}
V_{fg}
V_{tun}
I_{inj}
V_D
V_S=6V, V_D=0V
IHEI
CHHI+IHHI
Meas.
Model

Figure 2

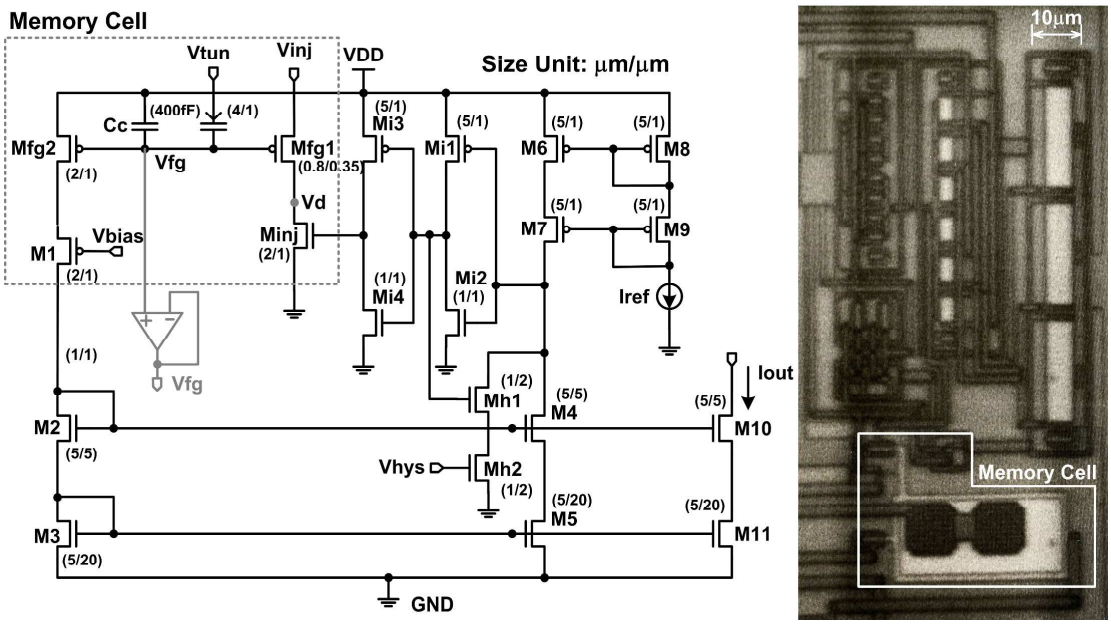
Memory Cell
Vtun
Vinj
VDD
Size Unit: μm/μm
(400fF)
(4/1)
Cc
Mfg2
(2/1)
Vfg
Mfg1
(0.8/0.35)
Vd
Vbias
M1
(2/1)
Minj
(2/1)
(5/1)
Mi3
Mi1
(5/1)
M6
(5/1)
M8
(5/1)
M7
(5/1)
M9
(1/1)
Mi4
Mi2
(1/1)
Iref
(1/1)
Vfg
(1/2)
Mh1
(5/5)
M4
(5/5)
M10
Iout
M2
(5/5)
Vhys
Mh2
(1/2)
(5/20)
M5
(5/20)
M11
M3
(5/20)
GND
10μm
Memory Cell

Figure 3

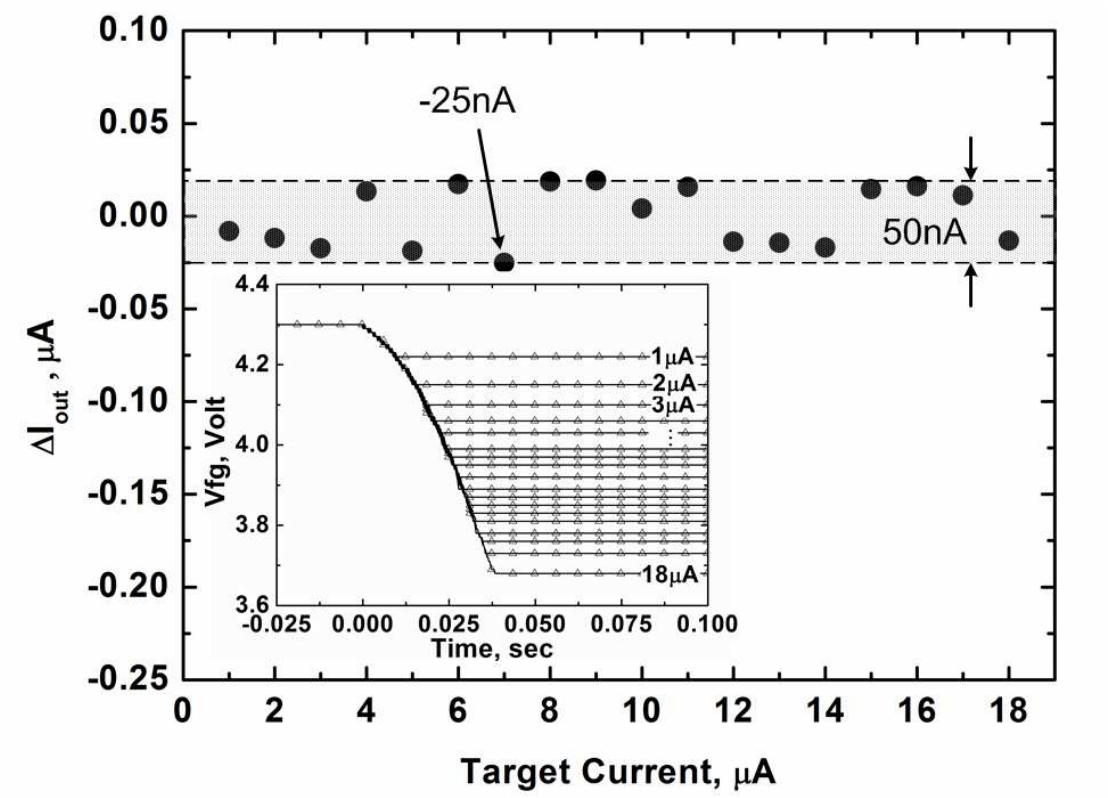
-25nA
50nA
ΔI_{out} , μA
Target Current, μA
Vfg, Volt
Time, sec
1μA
2μA
3μA
18μA

Figure 4