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Die-level, post-CMOS processes for fabricating open-gate, field-effect biosensor arrays with on-chip circuitry

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Abstract

Field-effect sensors have been applied extensively to numerous biomedical applications. To develop biosensor arrays in large scale, integration with signal-processing circuits on a single chip is crucial for avoiding wiring complexity and reducing noise interference. This paper proposes and compares two CMOS-compatible processes that allow open-gate, field-effect transistors (OGFETs) to be fabricated at the die level. The polygates of transistors are removed to maximize the transconductance. The CMOS compatibility further facilitates the monolithic integration with circuitry. Based on images and electrical measurements taken at different stages of the post-CMOS processes, a more feasible and reliable process is identified. The robustness of the fabricated OGFETs against the micromachining process and against moisture is further examined and discussed. Finally, the capability of the OGFETs in detecting ion concentrations, biomolecules, and electrophysiological signals is demonstrated.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Field-effect transducers have proved useful in a variety of biomedical applications, such as ion sensors or potentiometric sensors for neural recording [1–6]. In these applications, building biosensors into a large array is growing essential for detecting multiple biomolecules or for monitoring multiple neurons in parallel [7–9]. Following this trend, monolithic integration with on-chip circuitry becomes crucial to reduce wiring complexity and noise interference [6, 10]. There has thus been the development of field-effect sensors compatible with the complementary metal-oxide-semiconductor (CMOS) technology, the dominant integrated-circuit technology [11–13]. The compatibility with the standard CMOS process further facilitates the cost reduction and the massive production in commercial industry. However, the CMOS compatibility requires all micromachining processes to be carried out after the standard CMOS process and in constrained conditions (e.g., at low temperature) [11]. This makes it challenging to create customised structures or to coat application-specific materials on sensors. For example, coating inert metals such as platinum on electrode is essential for avoiding electrode oxidation or erosion caused by redox processes, while coating inert metal normally requires customised CMOS process which is costly.

Most CMOS-compatible, field-effect sensors [7, 14–16] thus simply employed the passivation layer (silicon nitride/silicon oxynitride) of the standard CMOS technology as both the surface material of sensors and the moisture insulator for the electronics underneath. A floating gate formed by metals and polygates was then used to couple potential changes at the sensory surface. Compared to the first ion-sensitive field-effect transistor whose gate is replaced by an aqueous solution [17], the floating-gate structure is helpful for reducing sensory drifts induced by ion absorption into the gate oxide, as well as the interference induced

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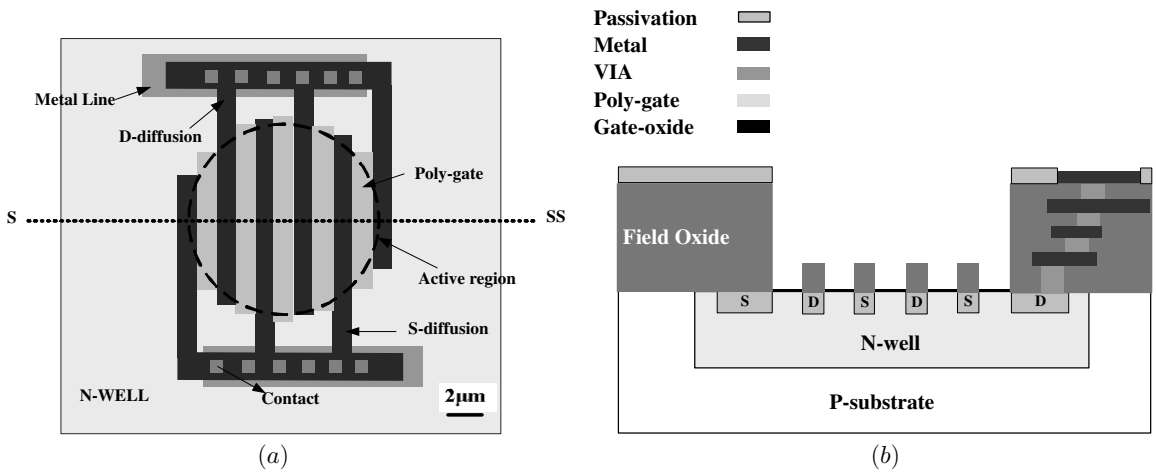

Figure 1. (*a*) The layout of a multifinger field-effect biosensor. (*b*) The cross-sectional view of the multifinger field-effect biosensor along the dashed line SS in (*a*).

by photo-currents. In contrast, the floating-gate structure together with the passivation layer separates the transistor distantly from the sensory surface, reducing significantly the coupling efficiency of potential changes at the sensory surface. Assume that the double-layer capacitance at the solution–solid interface is negligible. The coupling efficiency still depends on the ratio of the gate-oxide capacitance over the capacitance formed by the insulator between the solution and the floating gate. As the insulator (e.g., passivation) is much thicker than the gate oxide, a floating-gate area larger than several thousands of micrometre squares is normally required to guarantee a reasonable sensitivity. This consequently limits the spatial resolution of a sensory array, which is important for applications like neural recording, wherein a pitch size smaller than a single neuron (around 20 μm) is desirable [18]. In addition, the floating-gate structure introduces serious threshold-voltage variation because the residual charges on a floating gate can vary dramatically from one transistor to another [14, 15]. Procedures such as exposure to the UV-light is thus necessary to remove the residual charges before usage [15]. Therefore, variants such as the discrete-gate structure coated with a sensitive membrane [19, 20], or the field-effect transistors with gate omitted [21, 22], i.e. an open-gate structure, have been proposed. It is notable that the open-gate structure in [22] is created by plasma etching, which could damage the field-effect transistor easily or introduce extra mismatches, as will be discussed in this paper.

This paper proposes two post-CMOS processes for fabricating open-gate, field-effect transistors (OGFETs) at the die level. One process is based on wet etching, and the other on dry etching. Both processes remove the polygates and all materials above the sensing (active) region of the transistor, so that the field-effect transistor can interface with solutions through only its thin gate oxide (around 7 μm). The open-gate structure helps to enhance signal transduction and to avoid threshold variation suffered by field-effect sensors with a floating-gate structure. As coating photoresist evenly on a small die area is difficult, die-level fabrication is made possible by avoiding photolithography. This is especially important for designers who adopt the multi-wafer-project approach, by which they receive dies instead of a full wafer. In addition, the post-CMOS processes preserve metal layers for interconnection, allowing the field-effect sensors to form a two-dimensional array, as well as to integrate with signal-processing circuits on the same chip. For applications such as neural recording, this advance facilitates the development of open-gate 'neuro-transistor' arrays with a high spatial resolution, as has been infeasible with the open-gate transistor proposed by Fromherz *et al* [4, 9]. The technology proposed and demonstrated in this paper would thus point towards the development of a variety of field-effect biosensors with an open-gate structure in the standard CMOS technology.

Following the introduction, section 2 describes the design considerations and the post-CMOS processes for the OGFETs. With the two chips fabricated by the standard 0.35 μm CMOS technology of the Taiwan Semiconductor Manufacturing Company (TSMC), section 3 investigates the feasibility of the two post-CMOS processes. Based on device structures and electrical characteristics measured at different stages of the processes, a more reliable process flow is identified. The robustness of the fabricated OGFETs against the micromachining process and moisture is subsequently examined in section 4. Finally, the OGFET's capability in detecting ion concentrations, Deoxyribonucleic Acid (DNA), and electrophysiological signals is demonstrated in section 5.

2. Design of the field-effect biosensor

2.1. Layout and structure

Figure 1 shows the layout (top view) of the field-effect biosensor and its cross-sectional view along the line between S and SS. The dashed circle indicates the sensing (active) region of the transistor. Layout techniques for defining the active region will be detailed in the next subsection. The multifinger structure is employed to maximize the transconductance per unit area in the active region. To enhance signal transduction further, the polygate and the materials above are removed to form the open-gate structure, as shown in figure 1(*b*), while the gate oxide and metal wires are retained for circuit protection

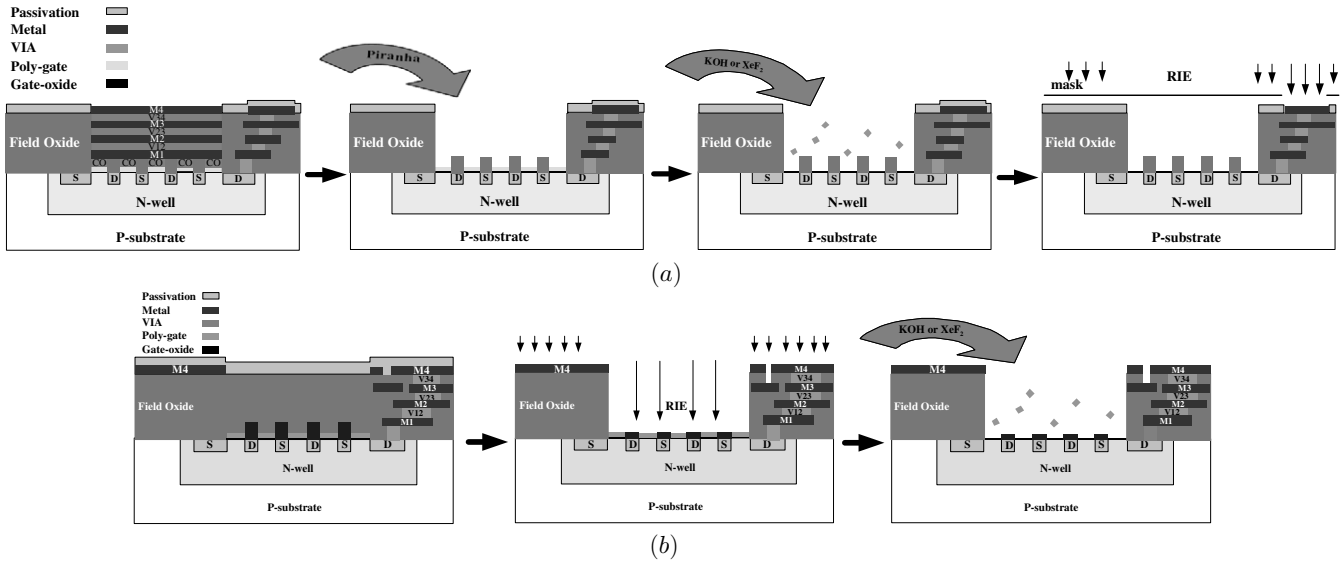

Figure 2. The micromachining process flow for fabricating the OGFETs in the standard CMOS technology. (*a*) The metal above the polygate is removed by wet etching with 'piranha'. (*b*) The field oxide above the polygate is removed by the reactive-ion etching.

and interconnection, respectively. Inside the active region with a diameter of 12 μm, the total W/L of the transistor is 50 μm/1 μm. It is notable that minimum linewidth is not adopted in order to ease the removal of polygates. In the TSMC 0.35 μm CMOS technology, the gate oxide is only 7 nm thick, greatly advantageous for the signal transduction.

2.2. *Post-CMOS process flow*

Figure 2 illustrates two possible methods of defining the active region and the corresponding process flows for removing materials above the gate oxide. In figure 2(*a*), stacks of metal layers are used to define the active region, and the metal layers are able to be removed by wet etching with 'piranha' (H_2SO_4:H_2O = 2:1) at 85 °C. All dies can be put together into the piranha using a tweezer and then rinsed by immersion in de-ionized water. In figure 2(*b*), the active region is defined by a shadow mask of one metal layer (M4), and the oxide above the active region is able to be removed by the reactive-ion etching (RIE). During RIE etching, the dies are stuck on the surface of a silicon wafer using copper tapes and then placed in the RIE chamber.

Both gate-exposure processes are simple but with potential drawbacks. The area of the VIA layer in figure 2(*a*) is much greater than the unique area (0.5 μm × 0.5 μm) regulated by the design rule. As VIA materials are deposited with constant amount in the standard CMOS process, violating the rule would result in underfilling of VIA materials, leading to the accumulation of impurity between VIA and metal layers. The impurity could then disrupt the etching of all metal layers. In contrast, the RIE attacks all materials except for metal, involving physical bombardments to device surfaces. The RIE is thus likely to introduce extra damage to the device. These potential drawbacks will be investigated in the next section.

After either of the gate-exposure processes, the silicide above the polygate is removed by the RIE for 5 min. Two possible methods are then applicable to removing the polygates (figure 2). One method is wet etching with diluted KOH (KOH:DI water = 1:2 by weight) at 80 °C, whose selectivity for polysilicon against oxide is more than 250 [23]. To protect the gate oxide and the full chip during KOH etching as much as possible, a tweezer can be used to handle the die so that only the die surface is in contact with the KOH solution. The other method is dry etching with XeF_2, whose selectivity for polysilicon against oxide is almost infinite [23]. While both methods have high selectivity, the gate oxide is only 7 nm thick in the TSMC 0.35 μm CMOS technology. It is important to examine which method preserves the thin oxide well.

The chip fabricated by the flow in figure 2(*a*) has its bonding pads protected by the passivation layer as the chip is returned from the foundry. After the gate-removal process, the passivation layer can be removed by the RIE etching, as shown in figure 2(*a*). Given pads placed in the periphery of the chip (figure 3), a simple mask such as the fragments of silicon wafers can be used to protect the field-effect sensors and on-chip circuitry during pad opening.

The two proposed process flows avoid photolithography, enabling the fabrication of OGFETs at the die level. In addition, metal layers are preserved for interconnection, facilitating the monolithic integration with signal-processing circuits, so as to reduce noise interference and routing complexity. It is notable that polygates can also be retained and coated with different materials to suit specific applications. On the other hand, if the sensor will be exposed to moisture for a long time, nitride compounds can be deposited on top of the gate oxide, while the transconductance of the sensor has to be compromised.

2.3. *Sensor arrays with integrated circuitry*

Figures 3(*a*) and (*b*) show the two chips fabricated with the TSMC 0.35 μm CMOS technology. Sensors in the chip in figure 3(*a*) are designed to be fabricated with the wet-etching process shown in figure 2(*a*), while sensors in the

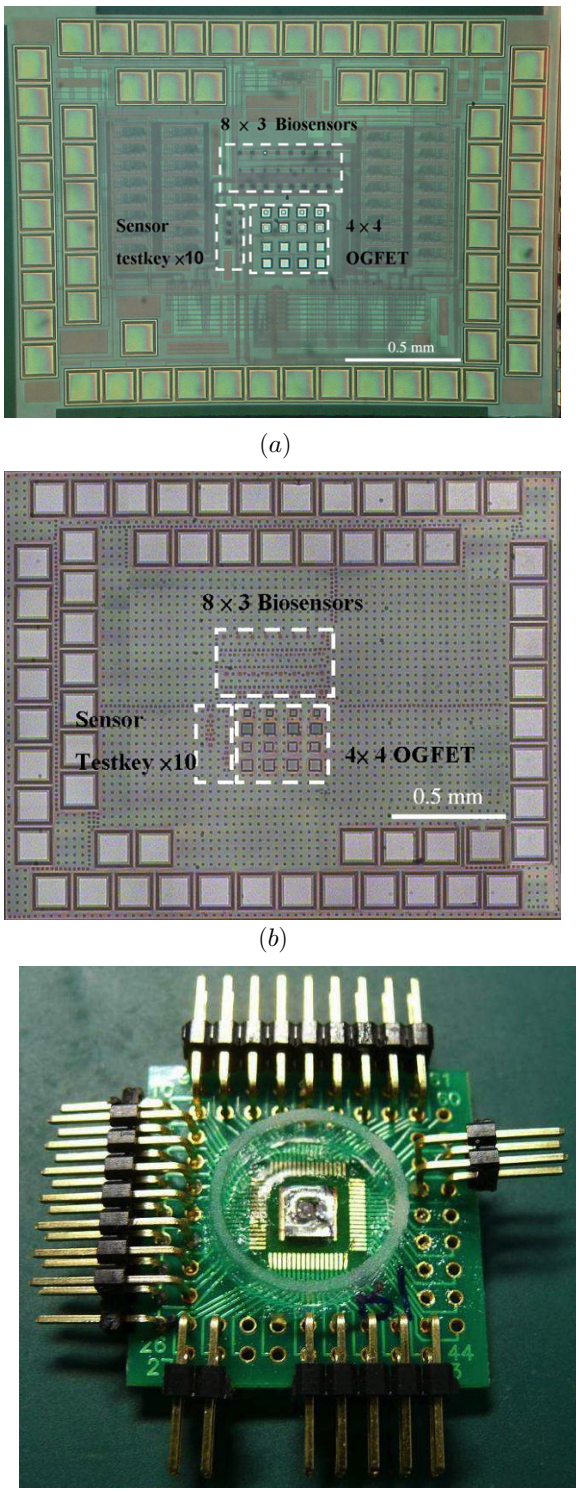

Figure 3. (*a*), (*b*) Microphotographs of the full chips whose field-effect biosensors will be fabricated with (*a*) the process flow in figure 2(*a*) and (*b*) the process flow in figure 2(*b*). (*c*) The packaged chip for electrical measurements and biological experiments.

chip in figure 3(*b*) with the dry etching process shown in figure 2(*b*). The chip in figure 3(*b*) therefore has all its surface, except for the active regions of sensors, covered by the metal mask. The sizes of the chips in figure 3(*a*) and (*b*) are 2.2 mm × 2.5 mm and 1.9 mm × 2.5 mm, respectively. Both chips contain two OGFET arrays, one with a circular active region and the other with a rectangular active region. The rectangular OGFETs have a large active region (20 μm × 20 μm) to facilitate monitoring the progress of micromachining processes. The circular OGFETs are integrated with preamplifiers and multiplexers, whose operation and measurement results have been detailed in [24]. In brief, the preamplifier uses a transistor with a feedback amplifier to form a low-impedance node, to which the drain of the OGFET is connected. All current changes of the OGFET induced by potential changes at its active region is thus directed into the transistor and then amplified by a simple current mirror. Finally, the amplified current is converted into a voltage signal by a current-to-voltage converter consisting of an operational amplifier and a tunable feedback resistor. By adjusting the biasing current and the feedback resistance, the gain of the full circuit can vary from 40 to 2000 (V/V). As the gain was set to be 400, the output noise measured in the absence of the sinusoidal signal was 17 mV_{RMS}, corresponding to an input-referred noise of 42.5 μV_{RMS}. This paper focuses on investigating the feasibility of the two proposed processes by scanning the structure of the rectangular OGFETs and by measuring the electrical characteristics of the circular OGFETs.

After post-CMOS processes, the chips were wire bonded to a printed-circuit board (PCB), to which a glass O-ring was attached to form a bath, as shown in figure 3(*c*). The entire chip surface except for the OSFET area was then coated with industrial epoxy (WK-8126H, WinKing) to prevent short circuits introduced by solutions in the bath. With an Ag/AgCl electrode immersed in the solution, the gate voltage of transistors was set through the electrode to facilitate all kinds of electrical measurements.

3. Fabrication

Figure 4 shows microphotographs of field-effect sensors taken at different stages of the post-CMOS processes. Figure 5 further shows the structural profiles of rectangular OGFETs scanned by the α-stepper. After gate-removal processes, the current–voltage (*I*–*V*) curves of multifinger OGFETs were measured, as shown in figure 6, indicating how well thin gate oxide was retained. The following subsections discuss these results and conclude a more reliable process flow.

3.1. Gate exposure by wet etching

Figure 4(*a*) shows photos of the OGFETs in the first chip (figure 3(*a*)) taken before gate-exposure process, after gate exposure by wet etching, and after gate removal by KOH etching. As the chip was returned from the foundry, the shining of metal layers above the active region of the OGFETs was clearly visible (the first column of figure 4(*a*)). The shining disappeared completely after the chip was immersed in piranha at 85 °C for 80 min (the second column of figure 4(*a*)). The obvious contrast indicates metal layers have been removed. Figure 5(*a*) shows the surface profiles of a rectangular OGFET scanned before and after the metal etching. The surface

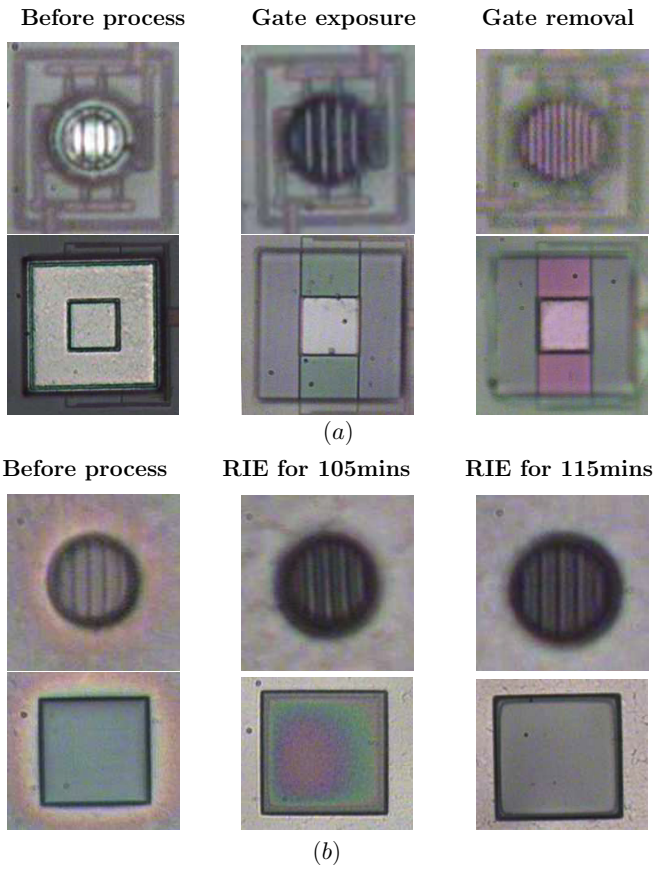

Figure 4. (*a*) Microphotographs of one multifinger and one rectangular OGFET taken during the process flow in figure 2(*a*). (*b*) Microphotographs of one multifinger and one rectangular OGFET taken during the process flow in figure 2(*b*).

exhibited a hole around 3 μm deep in the beginning due to the underfilling of VIA layers. After metal etching, the rectangular hole had a depth of around 7 μm[4], agreeing with the technology profile supplied by the TSMC. Complete removal of metal layers was thus confirmed. In addition, the underfilling of the VIA layers was proved to be harmless.

3.2. Gate exposure by RIE

Figure 4(*b*) shows photos of the OGFETs in the second chip (figure 3(*b*)) taken before and after the application of the RIE. The etching rate of the RIE was around 60 nm min^{-1}, and each run of the RIE last for 15 min in our experiment. To remove the oxide of 7 μm thick, eight runs of the RIE were applied. The second column in figure 4(*b*) shows the photos taken after the seventh run. The rainbow reflection revealed by the rectangular OGFET indicated that the oxide was almost etched completely. Therefore, the eighth run of the RIE was applied for only 10 min, and the reflection subsequently disappeared (third column in figure 4(*b*)). With the chip packaged, a complete removal of the oxide was further confirmed by examining whether the *I–V* curves of the transistor become measurable.

[4] The stair profile at around 6000 nm comes from the fact that only the CO layer is layout in the size of 20 μm × 20 μm, while other metal layers are in the size of 50 μm × 50 μm.

3.3. Gate removal by KOH etching

The etching rate of the KOH is greater than 10 000 Å min^{-1} for polysilicon, while less than 50 Å min^{-1} for the gate oxide [23]. The third column of figure 4(*a*) displays the photos of OGFETs taken after KOH etching for 20 s. The red-coloured regions correspond to the source/drain diffusions, while the regions in light-blue or light-red colours correspond to thin gate oxides. As visual observation was insufficient for indicating how well the gate-removal process was performed, the surface profiles of the rectangular OGFET were further scanned by the α stepper. As shown in figure 5(*a*), the difference between the profiles before and after the KOH etching indicates that around 200 nm thick of the polygate has been etched. To make sure the polygate was completely removed, the KOH etching was applied for different periods of times (10 s, 20 s, 30 s and 40 s), and the post-processed OGFETs were packaged as shown in figure 3(*c*) and measured. The OGFETs etched with KOH for more than 30 s were found to exhibit irregular *I–V* curves, most likely to result from the damage of the gate oxide. The optimum etching period was thus identified to be 20 s.

The *I–V* curves of a multifinger OGFET measured before and after the KOH etching are shown in figure 6(*a*), indicating the gate oxide has been well preserved during the gate-removal process. The transistor's threshold voltages before and after the KOH etching differ for two reasons. First, the work function of the new gate material, i.e. the solution in the bath (figure 3(*c*)), differs from that of polygates. Second, the gate oxide could be slightly etched, causing the threshold voltage and the transconductance to change. Over-etching gate oxide could further lead to variations across transistors, as shown in figure 6(*b*).

3.4. Gate removal by XeF_2 etching

The etching rate of XeF_2 is greater than 1100 Å min^{-1} for polysilicon, and almost zero for the gate oxide [23]. Figure 5(*b*) shows the surface profiles of the rectangular OGFET scanned after the polygate is dry-etched with XeF_2 for 1, 2 and 3 min. The depth of the rectangular hole increases by more than 300 nm after 1 min, and the increments become relatively smaller in the second and the third minutes. XeF_2 etching for 1 min is thus sufficient for removing the polygate. However, the *I–V* curves shown in figures 6(*c*) and (*d*) implies that the gate oxide has been damaged even in the first minute. The *I–V* curves of two identical OGFETs on the same die exhibit roughness after XeF_2 etching for 1 min, and become significantly irregular after XeF_2 etching for 2 min. In addition, the variations across transistors are considerably large. The unsatisfactory result is attributed to the DC bias added to enhance the XeF_2 etching in the reaction chamber. The DC bias may lead the XeF_2 plasma to attack the gate oxide physically, while the etching rate of XeF_2 may become difficult to control without the DC bias. Therefore, the XeF_2 etching is less favourable than the KOH etching for gate removal.

3.5. Discussion

In summary, experiment results indicate that wet etching with piranha and wet etching with KOH are favourable for

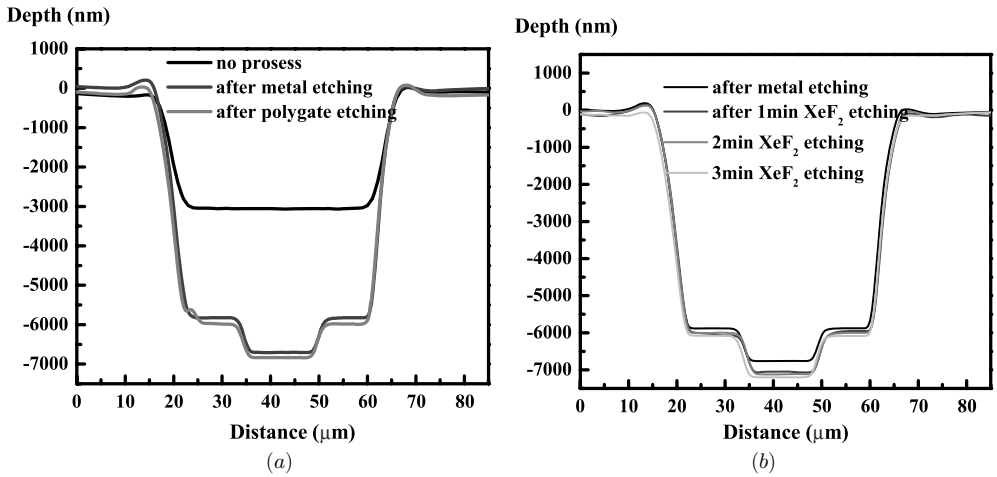

Figure 5. The surface profiles of rectangular field-effect biosensors scanned by α-stepper at different stages of the process flow in figure 2(*a*): (*a*) with KOH etching and (*b*) with XeF_2 etching.

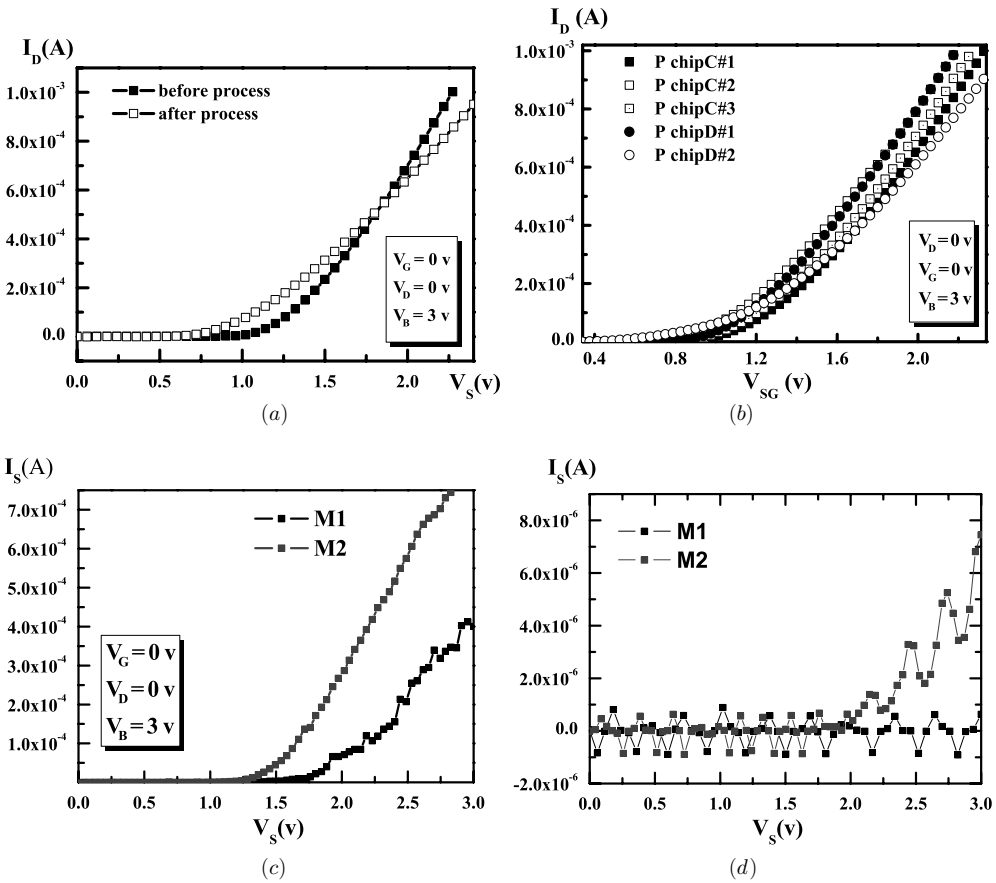

Figure 6. (*a*) The *I–V* curves of the multifinger transistor measured before and after the complete post-CMOS process in figure 2(*a*). The gate was removed by wet etching with KOH. (*b*) The *I–V* curves of different open-gate transistors on different dies. (*c*), (*d*) The *I–V* curves of two multifinger transistors (M1 and M2) measured after their polygates are removed by dry etching with XeF_2 for (*c*) 1 min (*d*) 2 min.

gate exposure and gate removal, respectively. The RIE and The XeF_2 etching are unfavourable because both processes involve more or less physical attacks to transistors, which can easily damage the thin gate oxide or introduce significant process variations. Figure 7 shows the scanning-electron-microscope (SEM) photo of a multifinger OGFET after the gate-removal process with KOH. The five rectangular grooves corresponding to five polygates are clearly revealed. The electrical characteristics of the multifinger OGFETs are further measured and discussed in the next section.

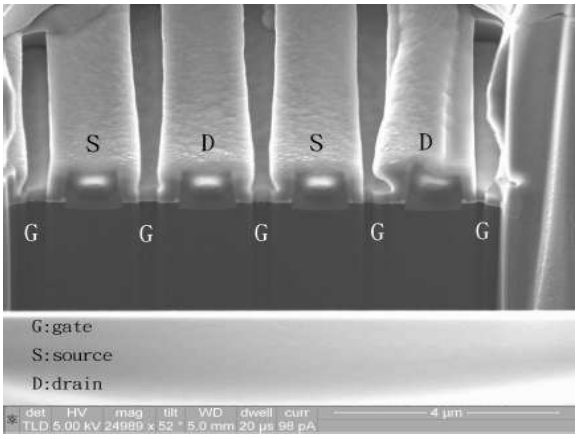

Figure 7. The scanning-electron-microscope photo of the multifinger OGFET which is cut in half by a focus-ion-beam system.

4. Electrical characteristics

4.1. Process variations

Micromachining processes, especially the gate-removal process, inevitably introduce extra process variations. Figure 6(*b*) shows the *I–V* curves of identical OGFETs distributed on two different dies. The variation across transistors is greater than that across dies, and the variation exists both in the threshold voltage and in the slope of the *I–V* curves. As both characteristics depend on the thickness of the gate oxide, this result implies that the post-CMOS process dominates to introduce the variation, resulting in gate oxides with a non-uniform thickness. Nevertheless, the variation has been much smaller than that exhibited by ion-sensitive field-effect transistors employing the floating-gate structure [14, 15]. The advantage of the open-gate structure is thus demonstrated. In addition, the variation can be largely eliminated with the calibration circuit proposed in [9], which sets the bias current and thus defines a unique transconductance for all transistors in an array.

4.2. Resistance to the moisture

Although OGFETs with thinner gate oxide is favourable for signal transduction, ions diffusing into the gate oxide can introduce non-negligible sensory drifts [25]. To test how well the proposed OGFET resists ion diffusions, the bath of the packaged chip was filled with physiological saline (210 mM NaCl; 15 mM CaCl2, 5.4 mM KCl, 2.6 mM MgCl2 and 5 mM HEPES, pH 7.4), and the *I–V* curves of a single OGFET were measured for four days. As shown in figure 8, the OGFET did exhibit sensory drifts, and the drifting direction varies from one to another day. Compared to the process variations shown in figure 6(*b*), the variation caused by ion diffusions is relatively smaller, and only the threshold voltages vary. The sensory drifts can thus be removed completely by the same calibration circuit proposed in [9]. In addition, such ion-induced sensory drift is likely to approach a constant value in the long term [25]. For applications preferring no drifts at all, thin films such as silicon nitride can be deposited over the gate oxide, while the transconductance will be compromised.

5. Biosensing capability

The OGFETs can function as a variety of biosensors, which transduce potential changes in the active region into changes in drain currents. The following section demonstrates the fabricated OGFET's capability to sense not only the static concentration of ions or biomolecules, but also dynamic electrophysiological signals in saline solutions.

5.1. Ion-concentration sensor

The OGFET's ability to sense ion concentrations was tested by filling NaCl solvents with different concentrations into the bath. Figure 9(*a*) shows the measured *I–V* curves of an OGFET in response to different NaCl solvents. With the concentration varying from 10^{-5} M to 1 M, the *I–V* curves shifted with a consistent step, corresponding to a consistent increment in the effective threshold voltage. This phenomenon came from the fact that the solvent with a higher

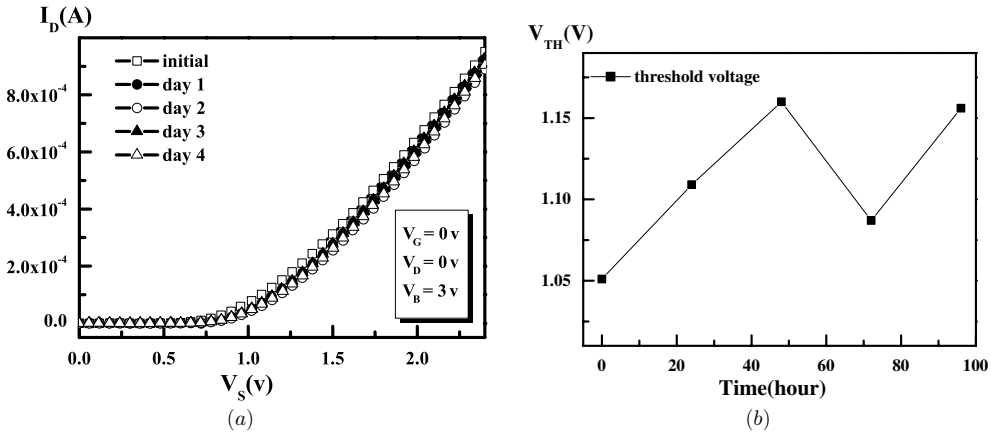

Figure 8. (*a*) The *I–V* curves and (*b*) the corresponding threshold voltages of an OGFET measured for four days, with physiological saline filled in the bath of the packaged chip.

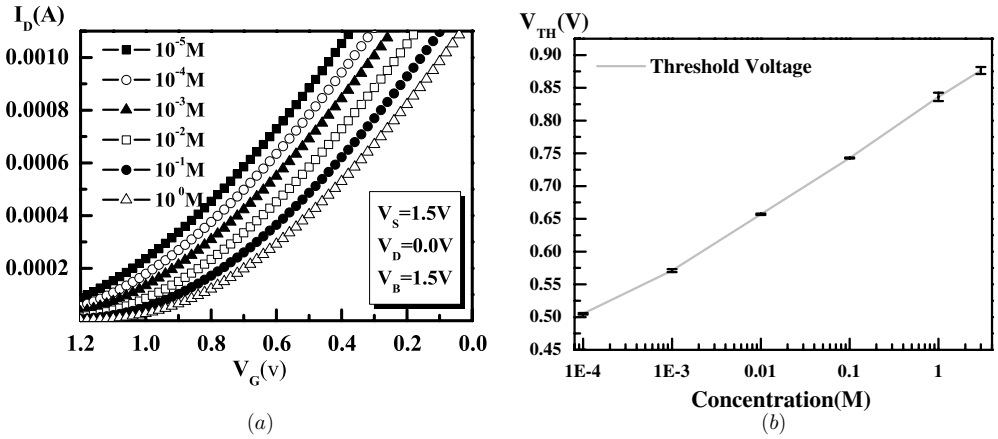

Figure 9. (*a*) The *I–V* curves of an OGFET in response to solvents with different NaCl concentrations. (*b*) The plot of NaCl concentration versus the effective threshold voltages extracted from the *I–V* curves of the OGFET. The grey curve indicates the average value over four experiments, and the error bars indicate corresponding standard deviations.

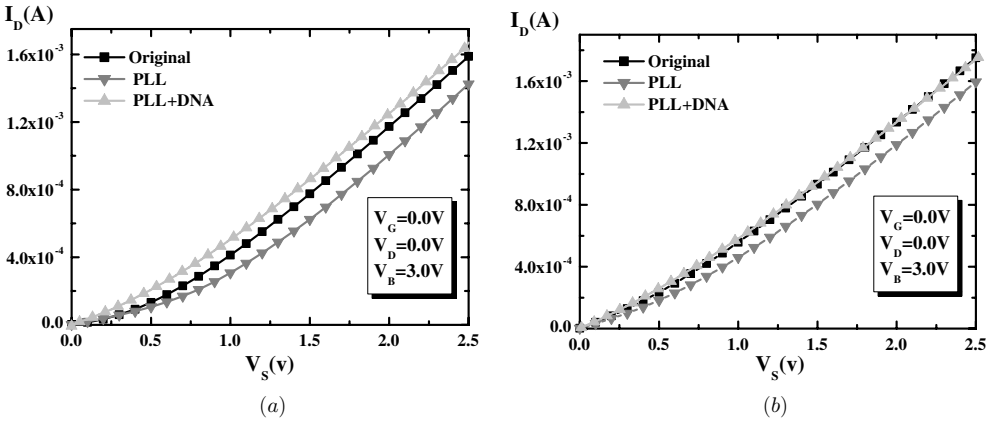

Figure 10. The *I–V* curves of two OGFETs measured when their sensory surfaces were bound with (1) nothing (square), (2) PLL (down triangle), and (3) PLL and DNA (up triangle).

ion concentration functioned as the gate material with a higher Fermi energy, leading to a higher threshold voltage for the p-type OGFET. Figure 9(*b*) plots the effective threshold voltage[5] against NaCl concentration. The grey curve indicates the average value over four experiments ($n = 4$), and the error bars display the corresponding standard deviations. Obviously, the OGFET possesses satisfactory linearity and reliability in terms of detecting ion concentrations.

5.2. Biomolecule detection

Deoxyribonucleic-Acid(DNA) microarrays has enabled the detection of gene expressions in a parallel and economic manner, wherein field-effect devices have proved to be one promising DNA sensor [26, 27], despite of the debate on detection mechanisms [28]. One mechanism relies on detecting the intrinsic charge of the DNA, while the other on the charge redistribution induced by DNA hybridization. Both mechanisms cause threshold voltages to change but in opposite directions. As suggested by [28], the DNA concentration on the sensory surface would determine which mechanism dominates.

Instead of coating single-strand DNA on the OGFET as probes to detect the hybridization of the DNA, a simpler experiment was carried out to test the OGFET's ability to detect the binding of double-strand DNAs onto the active region of the OGFET. The surface of the OGFET was first coated with the poly-L-lyseine (PLL) and dehydrated in room temperature. The PLL functioned as an interfacial material that promoted the binding of DNA to the surface of the OGFET. Afterwards, solution containing purely DNA segments of the Enhanced Green Fluorescent Protein (EGFP) was dropped onto the sensory region and then dehydrated in room temperature. The dehydration process ensured that only DNA segments were left and bound with the PLL on the chip surface. It is notable that the resultant DNAs on the chip surface are not different from that produced by the hybridization of single-strand DNAs. Figure 10 shows the *I–V* curves of two OGFETs measured (1) with nothing (2) with PLL and (3) with PLL and DNA bound on

[5] The effective threshold for each curve is extracted by deriving the tangent of the *I–V* curve at $I_D = 500\ \mu$A, extrapolating the tangent to intersect with the *x*-axis, and adopting the intersecting point as the threshold voltage.

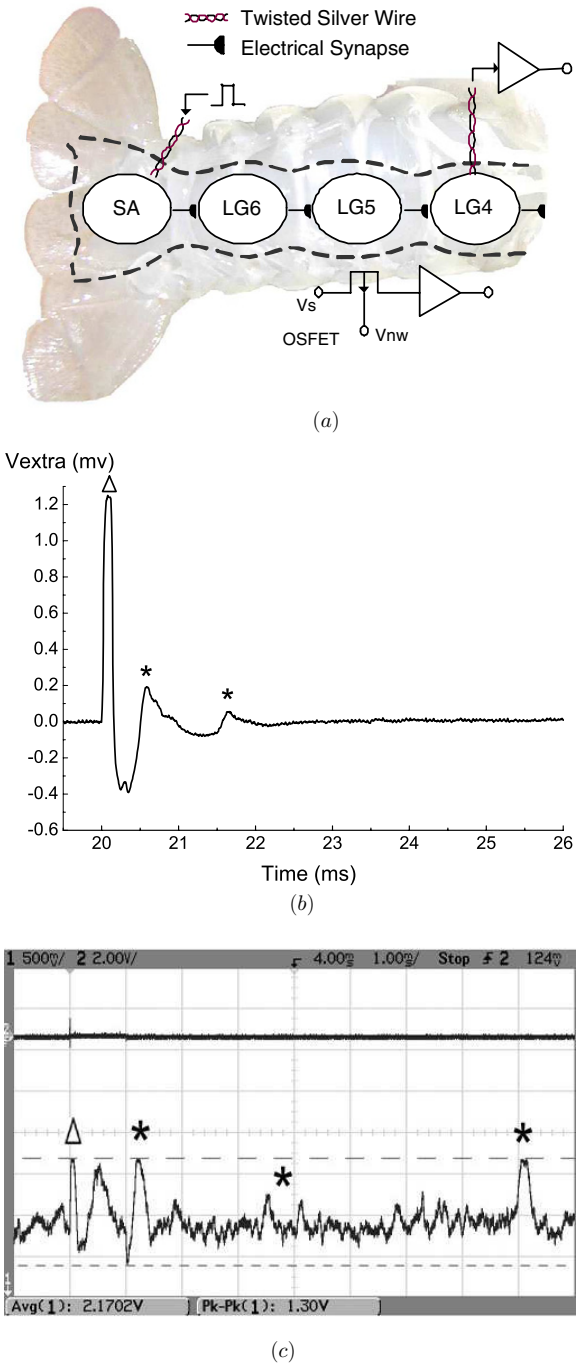

Figure 11. (*a*) Diagram illustrating the experimental setup with the escape neural circuit of the crayfish and its functionality. (*b*), (*c*) Neural activity of LG neurons recorded by (*b*) the silver wire and (*c*) the OSFET chip. The triangles denote stimulation artefacts, and asterisks the neural activity.

their sensory regions. All measurements were made by filling the bath with de-ionized (DI) water to set the gate voltage. As shown in figure 10, coating the PLL on the OSFETs all caused the *I–V* curves to shift rightwards, while the addition of DNA all caused the *I–V* curves to shift leftwards. Although the extent of curve shifting is different among transistors, the OGFET's capability in detecting the DNAs bound to the chip surface has been clearly demonstrated.

5.3. Recording electrophysiological signals

As the OGFET is inherently capable of detecting potential changes in the active region, OGFETs have been employed to record bio-potentials such as neural activity [4, 5, 24]. The chip's capability in recording electrophysiological signals was thus further experimented with the escape neural circuit of the crayfish [29–31]. The diagram in figure 11(*a*) illustrates the functionality of the escape circuit. The lateral giant (LG) neurons (LG6) receive inputs from the mechanosensory afferents (SA) in the tail. Once the afferents are stimulated simultaneously by the approach of a predator, LG6 neurons generate action potentials (APs) and propagate the APs to posterior LG neurons (LG5 and LG4) through electrical synapses. The sequential firings of LG neurons subsequently induce muscle contraction for the crayfish to escape from the predator.

Figure11(*a*) also illustrates the experimental setup. The nerve fibre of the crayfish, dissected less than 30 min was placed in the culturing bath with crayfish saline (210 mM NaCl; 15 mM CaCl2, 5.4 mM KCl, 2.6 mM MgCl2 and 5 mM HEPES, pH 7.4). One twisted, teflon-coated silver wire was employed to stimulate the sensory afferents extracellularly, while the other silver wire was used to record extracellularly the activity of the LG neurons. The signals recorded by the silver wire provide a credible reference for comparison with the signals recorded by the OSFET arrays. As a monophasic pulse with an amplitude of 5 V and a pulse width of 0.15 ms was applied to stimulate the sensory afferents extracellularly, an exemplary activity of LG neurons was recorded by another silver wire, as shown in figure 11(*b*). The large transient at the beginning is a stimulation artefact (marked with a triangle), whose duration agrees with the pulse width of the applied stimulation. The follow-up ripples thus correspond to the activation of LG neurons (marked with asterisks). A similar trace, as shown in figure11(*c*), was recorded by the OSFET chip. The on-chip recording circuit amplified the neural activity immediately into several hundreds of millivolts. The advantage of integrating signal-processing circuits on a single chip is thus demonstrated. In addition, the number of recorded activities increased dramatically, indicating that the activation of LG neurons posterior to those above the OSFET was also recorded.

6. Conclusion

Two post-CMOS processes for fabricating open-gate, field-effect transistors at the die level are proposed and realized. The more feasible and reliable process is identified to be the wet-etching approach. For gate exposure, using stacks of metals as sacrificial layers is proved to be a more reliable way of defining the active region of transistors. For gate removal, wet etching with diluted KOH is preferable than dry etching with XeF_2 because XeF_2-etching is found to damage the gate oxide easily. Electrical measurements of post-processed OGFETs

further indicate that the post-CMOS process dominates to introduce process variations, which are greater than the sensory drifts caused by ion diffusions into the gate oxide. Nevertheless, most of the variations can be eliminated by the calibration circuit proposed in [9]. Finally, the fabricated devices are shown capable of detecting ion concentrations, DNA strands, and dynamic potential changes in solutions. The proposed CMOS-compatible OGFET, therefore, facilitates the development of various types of field-effect biosensors in large scale, with signal-processing circuits integrated on a single chip.

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