A Necessary and Sufficient Closure Property for Two-Stage Constructions of Switching Networks

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***Abstract*—Two-stage constructions and banyan-type networks play important roles in designing high speed switch fabrics. Switch fabrics designed from two-stage constructions and banyan-type networks cannot realize all the permutations and are known as *conditionally nonblocking* switches. A renowned property for conditionally nonblocking switches is the *closure* property, i.e., *if all the switches in a two-stage construction can realize a subset of permutations that satisfy a certain property P, then the switch resulted from the two-stage construction can also realize a subset of permutations that satisfy the same property P.* However, such a closure property is mostly stated for the *sufficient* part in the literature and the necessary part of the statement is in general either not true or unknown. Finding such a *necessary* and *sufficient* result is of fundamental importance to two-stage constructions as it can completely characterize the permutations that are realizable by two-stage constructions.**

In this paper, we prove a *necessary* and *sufficient* closure property for two-stage constructions. For this, we consider uniform mapping permutations and define uniform mapping switches as switches that can only realize the set of uniform mapping permutations. We show that a switch constructed by a two-stage construction is a uniform mapping switch if and only if all the switches at the first stage and the second stage are uniform mapping switches. Such a necessary and sufficient result provides a complete characterization of the permutations that can be realized by two-stage constructions. Since banyan-type networks are constructed recursively by using two-stage constructions with 2×2 switches, we obtain a complete characterization for any realizable permutation of any banyan-type network as a composition of its trace, a uniform mapping permutation and its guide.

I. Introduction

A common method for constructing switches with a *large* number of inputs and outputs is to recursively interconnect switches with *small* numbers of inputs and outputs. In the literature (see e.g., the books [12], [3], [7]), there are two main approaches for doing this: (i) three-stage constructions and (ii) two-stage constructions. Three-stage constructions, including Clos networks [5] and Benes networks [1], are generally used for constructing *nonblocking* switches that can realize all the permutations. On the other hand, two-stage constructions, such as the X2 construction (a shuffle eXchange in front of a 2-stage interconnection network) and the 2X construction (a 2-stage interconnection network appended with a shuffle eXchange) in [12], [13], can only realize a subset of permutations (unless they are further horizontally expanded or vertically stacked like those in [16], [9]) and they are generally known as *conditionally nonblocking* switches. There are many conditionally nonblocking switches, e.g., compressors, decompressors, expanders, CU (Circular Unimodal) nonblocking switches [12], and each of them can realize a specific subset of permutations that satisfy a certain property. One of the most renowned properties for conditionally nonblocking switches is the *closure* property through a two-stage construction. For example, the X2 construction of CU nonblocking switches is also a CU nonblocking switch [12], i.e., if all the switches in the X2 construction are capable of realizing all the circular unimodal permutations, then the switch constructed from the X2 construction is also capable of realizing all the circular unimodal permutations. As banyan-type networks can be recursively constructed by using two-stage constructions with 2×2 switches, banyan-type networks are also conditionally nonblocking switches (from the closure property through a two-stage construction). In particular, it was shown in [12] that a banyan network preceded by a shuffle exchange is capable of realizing all the circular unimodal permutations.

Most of the closure properties for conditionally nonblocking switches through two-stage constructions in the literature are *sufficient* conditions, i.e., if all the conditionally nonblocking switches in a two-stage construction can realize a subset of permutations that satisfy a certain mathematical property P, then the conditionally nonblocking switch resulted from the two-stage construction can also realize a subset of permutations that satisfy the same property P. However, the necessary part of the statement is in general either not true or unknown, i.e., if all the conditionally nonblocking switches in a two-stage construction can realize a subset of permutations that satisfy a certain mathematical property P, then the conditionally nonblocking switch resulted from the two-stage construction can *only* realize a subset of permutations that satisfy the same property P. For instance, if all the switches in the X2 construction are capable of realizing all the circular unimodal permutations, then it is known that the switch resulted from the X2 construction is capable of realizing a strictly larger set of permutations than the set of circular unimodal permutations. As such, the set of circular unimodal permutations is only a strict subset of permutations realizable by a banyan network preceded by a shuffle exchange. Finding such a *necessary* and *sufficient* result is thus of fundamental importance to two-stage constructions as it completely characterizes the permutations that can be realized by two-stage constructions. For instance, if we construct an $NM \times NM$ switch by interconnecting M $N \times N$ *nonblocking* switches at the first stage and N $M \times M$ *nonblocking* switches at the second stage, then the total number

of permutations that can be realized by the $NM \times NM$ switch is $(N!)^M(M!)^N$. Then what is the mathematical property that characterizes these $(N!)^M(M!)^N$ permutations? If, furthermore, we recursively expand this two-stage construction into a multistage interconnection network, what is the mathematical property that characterize all the permutations that can be realized by this multistage interconnection network?

One of the main contributions of this paper is to prove a *necessary* and *sufficient* closure property for two-stage constructions. The key insight is to note that there is a unique routing path between an external input and an external output in a two-stage construction and thus all the inputs of a switch at the first stage must be mapped *uniformly* to the switches at the second stage. If we further recursively expand the switch into a multistage interconnection network by using two-stage constructions, then there is still a unique routing path between an external input and an external output and all the inputs of a switch at the first stage must be mapped *uniformly* to the switches in all the stages as a *banyan tree*. Permutations that satisfy this kind of property are called *uniform mapping* permutations in our previous work [4], where they were used for establishing the connections between fat-tree networks [11] and load-balanced switches [2], [15], [8], [10], [6]. Switches that can *only* realize uniform mapping permutations are then called *uniform mapping* switches in this paper. We show in Theorem 4 that an $NM \times NM$ switch constructed by interconnecting M $N \times N$ switches at the first stage and N $M \times M$ switches at the second stage is a uniform mapping switch if and only if all the switches at the first stage and the second stage are uniform mapping switches.

A *baseline* network [12] is a a banyan-type network recursively constructed by the two-stage construction with 2×2 switches. As an application of Theorem 4, we obtain in Corollary 6 that all the permutations realizable by a baseline network are uniform mapping permutations. This corollary can be shown to recover the result for the reverse-exchange network in Theorem 1 of [17]. A fundamental result for banyan-type networks is that they are all equivalent provided that port remappings are added for the external inputs and external outputs and these port remappings can be explicitly specified by *trace* and *guide* in [12]. In conjunction with such a result, we are able to obtain a complete characterization for the permutations that are realizable by a banyan-type network. These permutations can be represented as a composition of the trace of the banyan-type network, a uniform mapping permutation and the guide of the banyan network. Though there are characterizations of permutations realizable by *certain* banyan-type networks [17], our characterization seems to be the first complete characterization of the permutations realizable by *any* banyan-type network (to the best of our knowledge).

This paper is organized as follows. We introduce the two-stage construction in Section II and the uniform mapping property in Section III. In Section IV, we prove a necessary and sufficient result for the closure property through a two-stage construction. The connections to banyan-type networks are addressed in Section V, where we prove a complete characterization of all the permutations realizable by any banyan-type network. We conclude the paper in Section VI by addressing possible extensions of our work.

II. Two-stage Construction

In the section, we briefly review the 2-stage construction in the literature (see e.g., [12]).

An $N \times N$ switch is a network element that has N inputs and N outputs. Both inputs and outputs are indexed from $0, 1, \ldots, N-1$. An $N \times N$ permutation is a one-to-one mapping from $\{0, 1, \ldots, N-1\}$ to $\{0, 1, \ldots, N-1\}$. An $N \times N$ permutation σ is said to be *realizable* by an $N \times N$ switch if input i can be connected to output $\sigma(i)$ for all $i = 0, 1, \ldots, N-1$. An $N \times N$ switch is said to be *nonblocking* if all the $N!$ permutations are realizable.

Definition 1 (Two-stage construction) *A two-stage construction of an $NM \times NM$ switch, denoted by $2Stg(N, M)$, is constructed by interconnecting two stages of switches (as shown in Fig. 1), where the first stage consists of M $N \times N$ switches (indexed from 0 to $M-1$), and the second stage consists of N $M \times M$ switches (indexed from 0 to $N-1$). These two stages of switches are connected by the perfect shuffle or so-called shuffle exchange, i.e., the b^{th} output of the a^{th} switch at the first stage is connected to the a^{th} input of the b^{th} switch at the second stage. Also, index the NM inputs and outputs from 0 to $NM-1$. The NM inputs (resp., outputs) of the $NM \times NM$ switch are connected to the inputs of the switches at the first stage (resp., outputs of the switches at the second stage) directly. Specifically, the i^{th} input of the $NM \times NM$ switch is connected to the $x(i)^{th}$ input of the $a(i)^{th}$ switch at the first stage, where*

$$a(i) = \left\lfloor \frac{i}{N} \right\rfloor, \tag{1}$$

and

$$x(i) = i - a(i)N = i - N \left\lfloor \frac{i}{N} \right\rfloor, \tag{2}$$

for all $0 \le i \le NM-1$. Also, the o^{th} output of the $NM \times NM$ switch is connected to the $y(o)^{th}$ output of the $b(o)^{th}$ switch at the second stage, where

$$b(o) = \left\lfloor \frac{o}{M} \right\rfloor, \tag{3}$$

and

$$y(o) = o - b(o)M = o - M \left\lfloor \frac{o}{M} \right\rfloor, \tag{4}$$

for all $o = 0, 1, \ldots, NM-1$.

On the other hand, for given $x = 0, 1, \ldots, N-1$ and $a = 0, 1, \ldots, M-1$, the x^{th} input of the a^{th} switch at the first stage is the $i(a, x)^{th}$ input of the $NM \times NM$ switch with

$$i(a, x) = x + aN. \tag{5}$$

Similarly, for given $y = 0, 1, \ldots, M-1$ and $b = 0, 1, \ldots, N-1$, the y^{th} output of the b^{th} switch at the second stage is the $o(b, y)^{th}$ output of the $NM \times NM$ switch with

$$o(b, y) = y + bM. \tag{6}$$

One key property of the two stage construction is the *unique routing path property*, i.e., there is a unique routing path from an input to an output. For instance, suppose that we

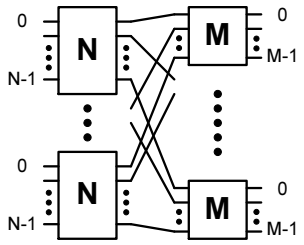

Fig. 1. An $NM \times NM$ $2Stg(N, M)$.

would like to connect the i^{th} input to the o^{th} output. Recall that the i^{th} input (of the $NM \times NM$ switch) is connected to the $x(i)^{th}$ input of the $a(i)^{th}$ switch at the first stage. The $a(i)^{th}$ switch at the first stage then connects its $x(i)^{th}$ input to its $b(o)^{th}$ output. Via the shuffle exchange between the two stages of switches, the $b(o)^{th}$ output of the $a(i)^{th}$ switch at the first stage is connected to the $a(i)^{th}$ input of the $b(o)^{th}$ switch at the second stage. The $b(o)^{th}$ switch at the second stage then connects its $a(i)^{th}$ input to its $y(o)^{th}$ output, which is exactly the o^{th} output of the $NM \times NM$ switch. We now take the routing path for the input/output pair $(i, o) = (1, 5)$ in a $2Stg(3, 2)$ as an example. According to (1), (2), (3) and (4), we have that $a(i) = 0$, $x(i) = 1$, $b(o) = 2$ and $y(o) = 1$. Then, the routing path can be written sequentially as follows: Input 1 of switch 0 at the first stage, output 2 of switch 0 at the first stage, input 0 of switch 2 at the second stage, and output 1 of switch 2 at the second stage. Fig. 2(a) shows the $2Stg(3, 2)$ and the routing path for input/output pair $(1, 5)$.

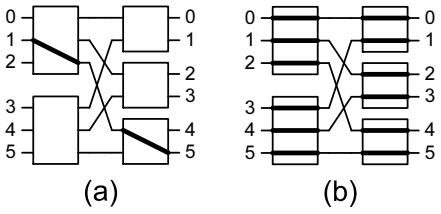

Fig. 2. (a) The routing path for the input/output pair $(1, 5)$ in a $2Stg(3, 2)$, and (b) the realization of the permutation σ in (9).

According to the unique routing property, for an arbitrary $NM \times NM$ permutation σ, one can determine the connection patterns in all the switches at both the first stage and the second stage. Specifically, for all the input/output pairs $\{(i, o)\}_{i=0}^{NM-1}$ with $o = o(i) = \sigma(i)$, the connection patterns $\{\sigma_{1,a}\}_{a=0}^{M-1}$ and $\{\sigma_{2,b}\}_{b=0}^{N-1}$ can be found as follows:

$$\sigma_{1,a(i)}(x(i)) = b(o), \tag{7}$$

for all $i = 0, 1, \ldots, NM - 1$, and

$$\sigma_{2,b(o)}^{-1}(y(o)) = a(i). \tag{8}$$

for all $o = 0, 1, \ldots, NM - 1$. Thus, there exist routing paths for all the input/output pairs if the a^{th} switch at the first stage connects input x to output $\sigma_{1,a}(x)$ for all $x = 0, 1, \ldots, N-1$ and $a = 0, 1, \ldots, M-1$ and the b^{th} switch at the second stage connects output y to input $\sigma_{2,b}^{-1}(y)$ for all $y = 0, 1, \ldots, M-1$ and $b = 0, 1, \ldots, N-1$. To ensure there is no conflict of these routing paths, i.e., all the routing paths are link disjoint (at the links of the shuffle exchange), the connection patterns $\{\sigma_{1,a}\}_{a=0}^{M-1}$ and $\{\sigma_{2,b}\}_{b=0}^{N-1}$ determined from the unique routing path property need to be permutations. As such, a $2Stg(N, M)$ can realize the $NM \times NM$ permutation σ if and only if (i) the connection patterns $\{\sigma_{1,a}\}_{a=0}^{M-1}$ (resp. $\{\sigma_{2,b}\}_{b=0}^{N-1}$) are all $N \times N$ (resp. $M \times M$) permutations, and (ii) these permutations $\{\sigma_{1,a}\}_{a=0}^{M-1}$ (resp. $\{\sigma_{2,b}\}_{b=0}^{N-1}$) can then be realized by the corresponding switches at the first (resp. second) stage.

In this paper, we focus on the class of the permutations that can be realized by the two-stage construction. We now consider a 2Stg(3,2) as shown in Fig. 2(b). Assume that all the 3×3 and 2×2 switches are nonblocking. Now we take the following permutation as an example:

$$\sigma = \begin{pmatrix} 0 & 1 & 2 & 3 & 4 & 5 \\ 0 & 2 & 4 & 1 & 3 & 5 \end{pmatrix}. \tag{9}$$

In order for σ to be realizable by such a network, the outputs of an arbitrary pair of inputs in $\{0, 1, 2\}$ cannot be in the same switch at the second stage. As a result, all the corresponding outputs of the 3 inputs of the 0^{th} switch at the first stage are needed to be mapped to all the 3 switches at the second stage, respectively. Also, all the inputs $3, 4, 5$ are needed to mapped to all the three switches at the second stage, respectively. One can easily verify that the permutation σ in (9) satisfies the conditions above. In general, for a $2Stg(N, M)$, a necessary condition for a permutation to be realizable is that all the N inputs in an arbitrary switch at the first stage are *bijectively* mapped to all the N switches at the second stage. The concept will be stated formally in Sections III and IV.

All the notations used for the two-stage construction are summarized in Table I.

TABLE I. LIST OF NOTATIONS.

$a(i)$	The switch at the first stage to which input i connects.
$b(o)$	The switch at the second stage to which output o connects.
$x(i)$	The input port of the $a(i)^{th}$ switch at the first stage to which input i connects.
$y(o)$	The output port of the $b(o)^{th}$ switch at the second stage to which output o connects.
$i(a, x)$	The input port to which the x^{th} input of the a^{th} switch at the first stage connects.
$o(b, y)$	The output port to which the y^{th} output of the b^{th} switch at the second stage connects.
$\sigma_{1,a}$	The connection pattern (mapping) needed to be realized in the a^{th} switch at the first stage for the permutation σ.
$\sigma_{2,b}$	The connection pattern (mapping) needed to be realized in the b^{th} switch at the second stage for the permutation σ.

III. UNIFORM MAPPING PROPERTY

For the n-vector $\mathbf{p} = (p_1, p_2, \ldots, p_n)$, we first defined $\{d_j^{\mathbf{p}}\}_{j=0}^{n}$ as

$$d_j^{\mathbf{p}} = \prod_{t=1}^{j} p_t, \tag{10}$$

where $d_0^{\mathbf{p}}$ is defined as $d_0^{\mathbf{p}} = 1$. In this paper, we let $N = \prod_{t=1}^{n} p_t = d_n^{\mathbf{p}}$. Then, we define the collection of sets $\{S^{\mathbf{p}}(j,k)\}_{j,k}$ as

$$S^{\mathbf{p}}(j,k) = \{x | k \cdot d_j^{\mathbf{p}} \leq x \leq (k+1)d_j^{\mathbf{p}} - 1\}, \tag{11}$$

for all $k = 0, 1, \ldots, N/d_j^{\mathbf{p}} - 1$ and $j = 0, 1, \ldots, n$. It is clear that

$$|S^{\mathbf{p}}(j,k)| = d_j^{\mathbf{p}}, \tag{12}$$

for all $k = 0, 1, \ldots, N/d_j^{\mathbf{p}} - 1$, $j = 0, 1, \ldots, n$. Moreover, according to the fact that $d_{j+1}^{\mathbf{p}} = \prod_{t=1}^{j+1} p_t = p_{j+1} d_j^{\mathbf{p}}$, the sets $\{S^{\mathbf{p}}(j,k)\}_{j,k}$ can be constructed recursively as

$$S^{\mathbf{p}}(j+1,k) = \bigcup_{\ell = k p_{j+1}}^{(k+1)p_{j+1}-1} S^{\mathbf{p}}(j,\ell), \tag{13}$$

for all $0 \leq j \leq n-1$. We now take $\mathbf{p} = (3,3,2)$ as an example. Then, for $j = 1$ and $k = 1$, we have from (10) that $d_{j+1}^{\mathbf{p}} = \prod_{t=1}^{2} p_t = 9$ and thus

$$S^{\mathbf{p}}(2,1) = \{x | 9 \leq x \leq 17\} = \{9, 10, \ldots, 17\}, \tag{14}$$

and $|S^{\mathbf{p}}(2,1)| = d_2^{\mathbf{p}} = 9$. Moreover, according to the fact $d_1^{\mathbf{p}} = p_1 = 3$ and $p_2 = 3$, one can verify that $S^{\mathbf{p}}(1,3) = \{9, 10, 11\}$, $S^{\mathbf{p}}(1,4) = \{12, 13, 14\}$, $S^{\mathbf{p}}(1,5) = \{15, 16, 17\}$ and

$$S^{\mathbf{p}}(2,1) = S^{\mathbf{p}}(1,3) \cup S^{\mathbf{p}}(1,4) \cup S^{\mathbf{p}}(1,5) \tag{15}$$

as shown in (13).

Also, for the n-vector $\mathbf{p} = (p_1, p_2, \ldots, p_n)$, we define the *reversed* vector of $\mathbf{p}$ as

$$r(\mathbf{p}) = (p_n, p_{n-1}, \ldots, p_1).$$

It is clear that the reversed vector of $r(\mathbf{p})$ is $\mathbf{p}$ itself:

$$r(r(\mathbf{p})) = (p_1, p_2, \ldots, p_n) = \mathbf{p}.$$

Moreover, according to (10), we have that

$$d_j^{r(\mathbf{p})} = \prod_{t=1}^{j} p_{n+1-t} = \prod_{n-j+1 \leq t \leq n} p_t = \frac{N}{d_{n-j}^{\mathbf{p}}}, \tag{16}$$

and $d_n^{r(\mathbf{p})} = d_n^{\mathbf{p}} = N$. We now define the *uniform mapping property* with respect to the vector $\mathbf{p} = (p_1, p_2, \ldots, p_n)$ as follows:

Definition 2 (Uniform mapping property) *Let $\mathbf{p} = (p_1, p_2, \ldots, p_n)$ and $N = \prod_{t=1}^{n} p_t$. For an $N \times N$ permutation σ and any set $S \subset Z_N = \{0, 1, \ldots, N-1\}$, $\sigma(S)$ is defined as the range of S, i.e.,*

$$\sigma(S) = \{y \in Z_N | y = \sigma(x) \text{ for some } x \in S\}.$$

A permutation σ is called to satisfy the $\mathbf{p}$-uniform mapping property or simply $\mathbf{p}$-uniform mapping if

$$|\sigma(S^{\mathbf{p}}(j,k)) \cap S^{r(\mathbf{p})}(n-j,\ell)| = 1, \tag{17}$$

for all $0 \leq j \leq n$, $k = 0, 1, \ldots, N/d_j^{\mathbf{p}} - 1$, and $\ell = 0, 1, \ldots, N/d_{n-j}^{r(\mathbf{p})} - 1$.

Note that $N/d_{n-j}^{r(\mathbf{p})} = d_j^{\mathbf{p}}$. The insight of the uniform mapping property in (17) is that the $d_j^{\mathbf{p}}$ inputs in the set $S^{\mathbf{p}}(j,k)$ are *uniformly* mapped to the $d_j^{\mathbf{p}}$ sets of outputs, $S^{r(\mathbf{p})}(n-j,\ell)$, $\ell = 0, 1, \ldots, d_j^{\mathbf{p}} - 1$. For an arbitrary $\mathbf{p}$-uniform mapping permutation σ, it is straightforward to versify that its inverse σ^{-1} is also uniform mapping corresponding to the reversed vector $r(\mathbf{p})$.

In the next section, we will address the relationship between the 2-stage construction of switching networks and the uniform mapping permutations. In particular, the permutations that can be realized by a 2-stage construction are uniform mapping permutations, and vice versa.

IV. Closure property for two-stage constructions

We first define the uniform mapping switch as the switches that can only realize all the uniform mapping permutations.

Definition 3 ($\mathbf{p}$-uniform mapping switch) *Let $\mathbf{p} = (p_1, p_2, \ldots, p_n)$ with $\prod_{t=1}^{n} p_t = N$. Then, an $N \times N$ switch is $\mathbf{p}$-uniform mapping if it can only realize all the $N \times N$ $\mathbf{p}$-uniform mapping permutations. In other words, an $N \times N$ permutation σ can be realized by an $N \times N$ $\mathbf{p}$-uniform mapping switch if and only if σ is $\mathbf{p}$-uniform mapping.*

We define the concatenation of an n-vector $\mathbf{p} = (p_1, p_2, \ldots, p_n)$ and an m-vector $\mathbf{q} = (q_1, q_2, \ldots, q_m)$ as

$$\mathbf{p} + \mathbf{q} = (p_1, p_2, \ldots, p_n, q_1, q_2, \ldots, q_m).$$

Then, it is clear that

$$r(\mathbf{p} + \mathbf{q}) = (q_m, \ldots, q_1, p_n, \ldots, p_1) = r(\mathbf{q}) + r(\mathbf{p}).$$

One of the main results of this paper is the following necessary and sufficient closure property for two-stage constructions.

Theorem 4 (A necessary and sufficient closure property for two-stage constructions) *Let $\mathbf{p} = (p_1, p_2, \ldots, p_n)$, $\mathbf{q} = (q_1, q_2, \ldots, q_m)$, $N = \prod_{t=1}^{n} p_t$ and $M = \prod_{t'=1}^{m} q_{t'}$. A $2Stg(N,M)$ is $\mathbf{p}+\mathbf{q}$-uniform mapping if and only if all the M $N \times N$ switches in the first stage are $\mathbf{p}$-uniform mapping and all the N $M \times M$ switches in the second stage are $\mathbf{q}$-uniform mapping.*

The proof for Theorem 4 uses the unique routing path property of the two-stage construction. Due to space limitation, the two-page proof of this theorem is not shown here and it can be found in the full technical report [14].

Note that, for $n = 1$, one can verify that all the $N \times N$ permutations are $\mathbf{p}$-uniform mapping with $p_1 = N$. Thus, for $n = 1$, an $N \times N$ nonblocking switch is also a uniform mapping switch. As a result, by using Theorem 4, we have the following corollary for the permutations that can be realized by the switching fabrics constructed recursively by nonblocking switches.

Corollary 5 *A recursive 2-stage construction switching fabric that uses nonblocking switches as building blocks is a $\mathbf{p}$-uniform mapping switch, where the vector $\mathbf{p}$ is determined*

by the sizes and the construction order of the nonblocking switches.

That is, only the uniform mapping permutations can be realized by the recursive 2-stage construction switching fabrics. Since the number of permutations that can be realized by a $p\times p$ nonblocking switch is $p!$, the total number of permutations that can be realized by a recursive 2-stage construction with nonblocking switches and the vector $\mathbf{p}$ is $\prod_{j=1}^{n}(p_j!)^{d_n^{\mathbf{p}}/p_j}$. As these permutations are $\mathbf{p}$-uniform mapping permutations, this also shows that the total number of $\mathbf{p}$-uniform mapping permutations is $\prod_{j=1}^{n}(p_j!)^{d_n^{\mathbf{p}}/p_j}$.

Later in Sec. V, we will show that all the banyan-type networks are variations of a recursive 2-stage construction switching fabric, where the building blocks are all 2×2 nonblocking switches, and we will use that to obtain a complete characterization of permutations that can be realized by any banyan-type network.

V. Characterization of Permutations in Banyan-Type Networks

A $2^n\times 2^n$ banyan-type network is a multistage interconnection network with n stages, indexed from 1 to n. Each stage consists of 2^{n-1} 2×2 switches, indexed from 0 to $2^{n-1}-1$. As there are two inputs and two outputs of a 2×2 switch, there are 2^n inputs and 2^n outputs at each stage. For each stage, index the first input (resp. output) and the second input (resp. output) of switch k as input (resp. output) $2k$ and input $2k+1$, respectively. To completely specify a banyan-type network, we need to describe how the 2^n outputs from one stage are connected to the 2^n inputs of the next stage. Let $(I_n(x), I_{n-1}(x),\ldots,I_1(x))$ be the binary representation of an integer $0\le x\le 2^n-1$, where $I_m(x)$ is the m^{th} least significant bit of x. Then, a banyan-type network is called a *baseline* network if, for $1\le j\le n-1$, output x of the j^{th} stage is connected to input y of the $(j+1)^{th}$ stage when y has the binary representation

$$(I_n(x), I_{n-1}(x),\ldots,I_{n-j+2}(x),\\ I_1(x), I_{n-j+1}(x), I_{n-j}(x)\ldots,I_2(x)).$$

Fig. 3 shows an 8×8 baseline network. In fact, Li [12, Theorem 3.5.12, pp.143] showed that a $2^n\times 2^n$ baseline network is a recursive 2-stage construction. For example, the 8×8 baseline network in Fig. 3 can be viewed as a $2Stg(2,4)$, and the 4×4 switch constructed by the 2×2 switches at second and third stages is also a 2-stage construction, $2Stg(2,2)$. Note that all the nonblocking switches used in a $2^n\times 2^n$ baseline network are all 2×2 switches. Hence, according to Corollary 5, a $2^n\times 2^n$ baseline network is a $\mathbf{p}$-uniform mapping switch where the elements in $\mathbf{p}$ are all 2. For the n-vector with all the elements being 2, it is clear that $\mathbf{p}=r(\mathbf{p})$ and $S^{\mathbf{p}}(j,k)=S^{r(\mathbf{p})}(j,k)$ for all $j=0,1,\ldots,n$, $k=0,1,\ldots,2^{n-j}$ and $n=1,2,\ldots$. To simplify the notations, we denote $S(j,k)=S^{\mathbf{p}}(j,k)$ if $p_t=2$ for all $t=1,\ldots,n$ in $\mathbf{p}$. Moreover, according to (11), the set $S(j,k)$ can be represented as

$$S(j,k)=\{x|k\cdot 2^j\le x\le (k+1)2^j-1\}, \tag{18}$$

for all j and k. Then, according to Theorem 4, a sufficient and necessary condition for the permutations that can be realized by baseline networks can be written as follows.

Corollary 6 *An arbitrary $2^n\times 2^n$ permutation σ can be realized by an $2^n\times 2^n$ baseline network if and only if the permutation satisfies the uniform mapping property, i.e.,*

$$|\sigma(S(j,k))\cap S(n-j,\ell)|=1, \tag{19}$$

for all $k=0,1,\ldots,2^{n-j}-1$, $\ell=0,1,\ldots,2^j-1$, $j=0,1,\ldots,n$, and $n=1,2,\ldots$, where the set $S(j,k)$ is defined as shown in (18).

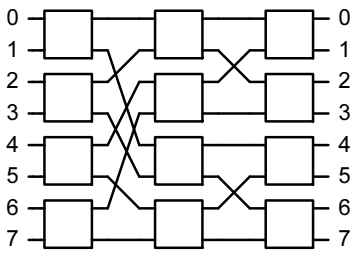

Fig. 3. An 8×8 baseline network.

We note that Wu and Feng obtained a complete characterization of the permutations realizable by the reverse-exchange network in Theorem 1 of [17]. By using the trace and guide transforms proposed by Li [12], one can verify that the baseline network and the reverse-exchange network [17] are equivalent with fixed input/output ports and thus they both can realize exactly the same set of permutations. As such, Corollary 6 recovers the result for the reverse-exchange network in Theorem 1 of [17].

Now we take one step further to obtain a complete characterization of permutations that can be realized by *any* banyan-type networks. Our approach is based on a fundamental result in Li's work [12] that showed an arbitrary pair of banyan-type networks can be made equivalent to each other with additional stages of input and output port remapping, where the remapping can be determined by their trace and guide transforms. In other words, each banyan-type network can be modified such that the modified banyan-type network is equivalent to the baseline network under cell rearrangement. According to Corollary 6, the modified banyan-type network can realize exactly the set of permutations satisfying the uniform mapping property. As such, one can determine the permutations in any banyan-type network by using the uniform mapping property and the trace and guide transforms of the banyan-type network as shown in the following theorem.

Theorem 7 (A complete characterization of permutations in a banyan-type network) *Let $N=2^n$ and $(I_n(x), I_{n-1}(x),\ldots,I_1(x))$ be the binary representation of $x\in Z_N$, where $I_m(x)$ is the m^{th} least significant bit of x. Consider an $N\times N$ banyan-type network with the trace transform $(t_1,t_2,\ldots,t_n)$ and the guide transform $(g_1,g_2,\ldots,g_n)$, respectively. Then, the permutation σ can be realized by the banyan-type network if and only if the permutation $(\sigma_{out}\circ\sigma\circ\sigma_{in})$ satisfies the uniform mapping property as shown in (19), where the permutations σ_{in} and σ_{out} are defined as*

$$I_{n+1-t_m}(\sigma_{in}(x))=I_m(x), \tag{20}$$

and

$$I_{n+1-m}(\sigma_{out}(x))=I_{n+1-g_m}(x), \tag{21}$$

for all $x \in Z_N$ *and* $m = 1, 2, \ldots, n$.

Proof. For the banyan-type network with the trace transform $(t_1, t_2, \ldots, t_n)$ and the guide transform $(g_1, g_2, \ldots, g_n)$, respectively, we now append additional stages of the input and output port remapping σ_{in} and σ_{out} such that the modified banyan-type network is equivalent to the $N \times N$ baseline network. We now claim that the permutations σ_{in} and σ_{out} can be determined *uniquely* according to the trace and guide transforms of the original banyan-type network. Then, according to Corollary 6, the following conditions are equivalent to each other: (i) The permutation σ can be realized by the original banyan-type network, (ii) the permutation $\sigma_{out} \circ \sigma \circ \sigma_{in}$ can be realized by the modified banyan-type network, i.e., the baseline network, and (iii) the permutation $\sigma_{out} \circ \sigma \circ \sigma_{in}$ satisfies the uniform mapping property.

We first consider σ_{in}, the input port remapping. Recall that, for the banyan-type network with the trace transform $(t_1, t_2, \ldots, t_n)$, the n^{th} most significant bit of the input of the m^{th} stage is the ${t_m}^{th}$ most significant bit of the input of the banyan-type network. Also, according to [12, Table 4.1], the trace transform of a baseline network is $(n, n-1, \ldots, 1)$ and thus the n^{th} most significant bit of the input of the m^{th} stage is the $(n+1-m)^{th}$ most significant bit of the input of the baseline network. Since the objective of the additional input port remapping σ_{in} is to transfer the trace transform from $(n, n-1, \ldots, 1)$ to $(t_1, t_2, \ldots, t_n)$, for an arbitrary number $x \in Z_N$, one should make the $(n+1-m)^{th}$ most significant bit of x be equal to the ${t_m}^{th}$ most significant bit of $\sigma_{in}(x)$ for all $m = 1, 2, \ldots, n$ as shown in (20), where $I_m(x)$ is the m^{th} *least* significant bit of x. On the other hand, for the banyan-type network with the guide transform $(g_1, g_2, \ldots, g_n)$, the n^{th} most significant bit of the output of the m^{th} stage is the ${g_m}^{th}$ most significant bit of the output of the banyan-type network. Again, the additional output port remapping σ_{out} transfers the guide transform from $(g_1, g_2, \ldots, g_n)$ to $(1, 2, \ldots, n)$, which is the guide transform of the baseline network [12, Table 4.1]. Hence, for an arbitrary $x \in Z_N$, we have that the ${g_m}^{th}$ most significant bit of x equals the m^{th} most significant bit of $\sigma_{out}(x)$ as shown in (21).

■

VI. Conclusion

In this paper, we proved two main results: (i) an $NM \times NM$ switch constructed by interconnecting M $N \times N$ switches at the first stage and N $M \times M$ switches at the second stage is a uniform mapping switch if and only if all the switches at the first stage and the second stage are uniform mapping switches, and (ii) any permutation that is realizable by a banyan-type network can be written as a composition of its trace, a uniform mapping permutation and its guide. The complete characterization of all the permutations that can be realized by a banyan-type network can provide a unified way to prove various conditionally nonblocking properties for banyan-type networks. For instance, it is known that a banyan network preceded by a shuffle exchange can realize all the circular unimodal (CU) permutations [12]. Such a result can be shown directly by mapping the set of CU permutations to a subset of uniform mapping permutations.

Acknowledgment

This work was supported in part by Ministry of Science and Technology (MOST), Taiwan, under Grant Numbers 102-2221-E-007 -006 -MY3, 103-2622-E-009-012 and 103-2218-E-007 -022.

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