Optimal Constructions of Fault Tolerant Optical Linear Compressors and Linear Decompressors

Cheng-Shang Chang, *Fellow, IEEE*, Jay Cheng, *Member, IEEE*, Tsz-Hsuan Chao, *Student Member, IEEE*, and Duan-Shin Lee, *Senior Member, IEEE*

***Abstract*—The constructions of optical queues is one of the most critically sought after optical technologies in all-optical packet-switched networks, and constructing optical queues directly via optical Switches and fiber Delay Lines (SDL) has received a lot of attention recently in the literature. A practical and challenging issue in the constructions of optical queues is on the fault tolerant capability of such constructions. In this paper, we focus on the constructions of fault tolerant optical linear compressors and linear decompressors. The basic network element for our constructions is scaled optical memory cell, which is constructed by a 2×2 optical crossbar switch and a fiber delay line.**

We first obtain a fundamental result on the minimum construction complexity of a linear compressor by using fiber delay lines as the storage devices for the packets queued in the linear compressor. This result shows that one of our previous constructions of a linear compressor by a concatenation of scaled optical memory cells is an optimal construction in the sense of minimizing the construction complexity. However, such an optimal construction lacks the fault tolerant capability. To construct a linear compressor with fault tolerant capability, we give a multistage construction of a *self-routing* linear compressor by a concatenation of scaled optical memory cells, and show that if the delays, say $d_1, d_2, \ldots, d_M$, of the fibers in the scaled optical memory cells satisfy a certain condition (specifically, the condition in (A2) given in Section IV-A), then our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ in the worst case even after up to F of the M scaled optical memory cells fail to function properly, where $0 \le F \le M-1$. Furthermore, we prove that our multistage construction with the fiber delays $d_1, d_2, \ldots, d_M$ given by the generalized Fibonacci sequence of order F is the best among all of the constructions of a linear compressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells. Similar results are also obtained for the constructions of fault tolerant linear decompressors.

***Index Terms*—Fault tolerant capability, linear compressors, linear decompressors, optical queues, switched delay lines.**

This research was supported in part by the National Science Council, Taiwan, R.O.C., under Contract NSC-93-2213-E-007-040, Contract NSC-93-2213-E-007-095, Contract NSC-94-2213-E-007-046, and the Program for Promoting Academic Excellence of Universities NSC 94-2752-E-007-002-PAE. This paper was presented in part at the IEEE International Conference on Computer Communications (INFOCOM'07), Anchorage, AK, USA, May 6–12, 2007.

Cheng-Shang Chang and Tsz-Hsuan Chao are with the Institute of Communications Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C. (e-mail: cschang@ee.nthu.edu.tw; thchao@gibbs.ee.nthu.edu.tw).

Jay Cheng is with the Department of Electrical Engineering and the Institute of Communications Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C. (e-mail: jcheng@ee.nthu.edu.tw).

Duan-Shin Lee is with the Department of Computer Science and the Institute of Communications Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C. (e-mail: lds@cs.nthu.edu.tw).

I. Introduction

One of the key problems of optical packet switching is the lack of optical queues as optical packets cannot be easily stopped, stored, and forwarded, and it is well recognized that one of the most critically sought after technologies in all-optical packet switching is the constructions of optical queues for contention resolution among packets competing for the same resources in the optical domain. The only known way to "store" optical packets without converting them into other media is to direct them via a set of optical switches through a set of fiber delay lines so that the optical packets come out at the right place and at the right time. As such, it has been recognized that constructing optical queues directly via optical Switches and fiber Delay Lines (SDL) is one of the promising technologies for the design of optical queues, and the SDL constructions of optical queues have received a lot of attention recently in the literature (see e.g., [1]–[29] and the references therein).

Early SDL constructions for optical queues, including the "shared-memory optical packet switch" in [1], the "staggering switch" in [2], "quadro-star" in [3], and "CORD (contention resolution by delay lines)" in [4], focused more on the feasibility of such an approach through numerical simulations. Recently, theoretical advances in the SDL constructions have shown that there exist systematic methods for the constructions of various types of optical queues, including output-buffered switches in [5]–[9] and [13], first-in first-out (FIFO) multiplexers in [5] and [10]–[15], FIFO queues in [16] and [17], last-in first-out (LIFO) queues in [17], priority queues in [18]–[20], and linear compressors, non-overtaking delay lines, and flexible delay lines in [21] and [22]. More recent results on the theoretical SDL constructions of optical queues can be found in [23]–[26]. For review articles on the SDL constructions of optical queues, we refer to [27]–[29] and the references therein.

A practical and challenging issue in the constructions of optical queues is on the fault tolerant capability of such constructions, which deals with the situation that some of the components of a network element may not function properly. Without taking the reliability aspect into consideration during the design process, even a single faulty component within a network element consisting of hundreds or thousands of components can lead to a total breakdown of the entire network element. As such, the constructions of fault tolerant network elements are extremely important and challenging from a practical point of view.

In this paper, we focus on the constructions of fault tolerant optical linear compressors and linear decompressors. As in most works in the SDL literature, we assume that packets are of the same size. Furthermore, time is slotted and synchronized so that every packet can be transmitted within a time slot. By so doing, packets can be "stored" in a fiber delay line with the propagation delay being an integer multiple of a time slot.

We will use scaled optical memory cells as basic network elements for the constructions of fault tolerant linear compressors and linear decompressors. A scaled optical memory cell that will be described in detail in Section II is constructed by a 2×2 optical crossbar switch and a fiber delay line. In Section II, we obtain a fundamental result on the minimum construction complexity of a linear compressor by using fiber delay lines as the storage devices for the packets queued in the linear compressor. This result shows that our previous construction of a linear compressor by a concatenation of scaled optical memory cells in [21] is an optimal construction in the sense of minimizing the construction complexity. However, such an optimal construction lacks the fault tolerant capability. To construct a linear compressor with fault tolerant capability, we first show a two-stage construction of a linear compressor in Section III. Such a two-stage construction is recursively expanded to give a multistage construction of a *self-routing* linear compressor by a concatenation of M scaled optical memory cells. We obtain a condition (specifically, the condition in (A1) given in Section III-B) on the delays $d_1, d_2, \ldots, d_M$ of the fibers in the M scaled optical memory cells so that our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M} d_i$. Then in Section IV, we use (A1) to show a more general condition (specifically, the condition in (A2) given in Section IV-A) on the delays $d_1, d_2, \ldots, d_M$ so that our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ in the worst case even after up to F of the M scaled optical memory cells are broken. Furthermore, we show an optimality result that our multistage construction with the fiber delays $d_1, d_2, \ldots, d_M$ given by the generalized Fibonacci sequence of order F is the best among all of the constructions of a linear compressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells. Similar results for the constructions of fault tolerant linear decompressors are given in Section V. Finally, we conclude this paper in Section VI.

II. An Optimal Construction of a Linear Compressor

In our previous papers [16] and [21], we used optical memory cells as basic network elements for the constructions of various types of optical queues. An optical memory cell (see Figure 1) is constructed by a 2×2 optical crossbar switch and a fiber delay line with one time slot (unit) of delay. To write a packet to the optical memory cell, set the 2×2 crossbar switch to the "cross" state so that the packet at the input link can be directed to the fiber delay line with one time slot of delay. Once the write operation is completed, the crossbar switch is then set to the "bar" state so that the packet directed into the fiber delay line keeps recirculating through the fiber delay line. To read out the information from the optical memory cell, set the crossbar switch to the "cross" state so that the packet in the fiber delay line can be directed to the output link.

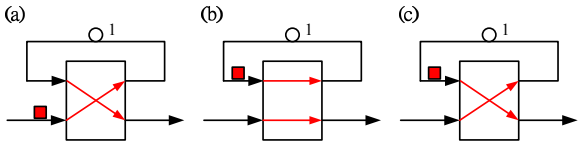


Fig. 1. An optical memory cell: (a) writing information (b) recirculating information (c) reading information.

A scaled SDL element is said to be with scaling factor m if the delay of every delay line is m times of that in the original (unscaled) SDL element. One of the most important properties of SDL elements is the time interleaving property for scaled SDL elements in [10]: a scaled SDL element with scaling factor m can be operated as the time interleaving of m (unscaled) SDL elements. For example, in Figure 2, we show a scaled optical memory cell with scaling factor 2 as the length of the delay line in Figure 2 is twice of that in the original (unscaled) optical memory cell in Figure 1. To operate a scaled optical memory cell with scaling factor 2 as the time interleaving of two (unscaled) optical memory cells, one first partitions time into odd and even numbered time slots. For the odd numbered time slots, one can set the connection patterns of the 2×2 optical crossbar switch in the scaled SDL element according to the read/write operation for one memory cell. Similarly, for the even numbered time slots, one can set the connection patterns of the 2×2 optical crossbar switch in the scaled SDL element according to the read/write operation for another memory cell. Intuitively, a scaled optical memory cell with scaling factor m is capable of storing m packets. However, the packets stored in a scaled optical memory cell cannot be accessed in an arbitrary manner as that of a random access memory (RAM); instead, they can only be accessed "one at a time" in a sequential manner. This is because only the packet at the head of the fiber delay line (that is connected to the upper input link of the 2×2 switch) in the scaled optical memory cell can be accessed during each time slot, while the other packets keep moving forward inside the fiber delay line and cannot be accessed until they appear at the head of the fiber delay line.

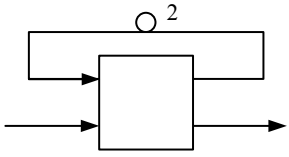


Fig. 2. An optical memory cell with scaling factor 2.

Now we review the definition of a linear compressor and the construction of a linear compressor by a concatenation of scaled optical memory cells in [21].

Definition 1 (Linear compressors [21]) *Suppose that the departure time of a packet is known upon its arrival. Let*

$\tau^a(n)$ and $\tau^d(n)$ be the arrival time and the departure time, respectively, of the n^{th} packet. A network element with a single input link and a single output link is called a linear compressor *with the range of delay $[d_1, d_2]$ if it realizes the set of mappings that satisfy*

$$\tau^a(n) + d_1 \leq \tau^d(n) \leq \tau^a(n) + d_2 \text{ for all } n, \quad (1)$$

and the following monotone and consecutive condition:

$$\tau^d(n) = \tau^d(n-1) + 1 \text{ whenever } \tau^a(n) \leq \tau^d(n-1). \quad (2)$$

In particular, if $d_1 = 0$, then it is called a linear compressor with maximum delay d_2.

As pointed out in [21], the name, linear compressor, originates from its counterpart for space switches (see e.g., [30] and [31]). The condition $\tau^a(n) \leq \tau^d(n-1)$ means that the n^{th} packet arrives before the $(n-1)^{th}$ packet departs. If one defines a busy period of a linear compressor as the period of time that there are packets in the linear compressor, then the monotone and consecutive condition implies that the departures in a busy period are monotone and consecutive (see the sample path of a linear compressor in Figure 3 for an illustration). Note that the packet initiating a busy period can have an arbitrary delay (as long as its delay is not greater than the maximum delay of the linear compressor).

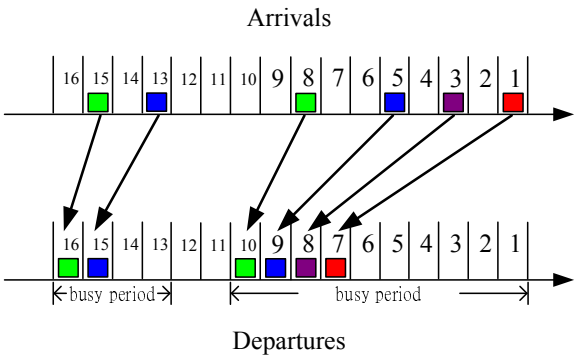


Fig. 3. A sample path of a linear compressor with maximum delay d, where $d \geq 6$.

It was shown in [21] that a linear compressor with maximum delay $2^M - 1$ can be constructed by a concatenation of M scaled optical memory cells with scaling factors $1, 2, 2^2, \ldots, 2^{M-1}$ in Figure 4. Moreover, such a construction is a self-routing linear compressor. Specifically, let $x = \tau^d(n) - \tau^a(n)$ be the delay of the n^{th} packet, and let the M-vector $(b_1(x), b_2(x), \ldots b_M(x))$ be the binary representation of x (from the least significant bit to the most significant bit), i.e., $x = \sum_{i=1}^{M} b_i(x)2^{i-1}$. If the M scaled optical memory cells are indexed $1, 2, \ldots, M$ from left to right, then the n^{th} packet is routed to the fiber delay line with delay 2^{i-1} in the i^{th} scaled optical memory cell only if $b_i = 1$. We note that the two-stage construction of a linear compressor in [21] is analogous to the "2X version" of a two-stage interconnection network in [31].

In the following theorem, we show a fundamental result on the minimum construction complexity of a linear compressor

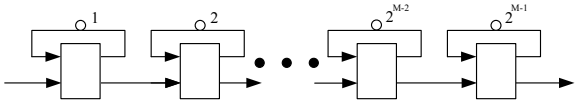


Fig. 4. A self-routing linear compressor with maximum delay $2^M - 1$.

by using fiber delay lines as the storage devices for the packets queued in the linear compressor.

Theorem 2 *Suppose that a linear compressor with maximum delay d is constructed by using SDL elements that contain M fiber delay lines as the storage devices for the packets queued in the linear compressor. Then*

$$d \leq 2^M - 1, \quad (3)$$

or, equivalently,

$$M \geq \lceil \log_2(d+1) \rceil. \quad (4)$$

In other words, the minimum construction complexity in terms of the number of fiber delay lines needed as the storage devices for the construction of a linear compressor with maximum delay d is $\lceil \log_2(d+1) \rceil$.

Proof. Let $d_1 \leq d_2 \leq \cdots \leq d_M$ be the delays of the M fiber delay lines in the linear compressor. Note that $d_1 = 1$. Otherwise, if $d_1 > 1$, then a packet with delay equal to 1 cannot depart at its departure time as this packet must be stored in one of the fibers and the delay of every fiber delay line is greater than 1 in this case.

Let $j = \max\{1 \leq j' \leq M : d_{k+1} \leq \sum_{i=1}^{k} d_i + 1 \text{ for all } k = 0, 1, \ldots, j'-1\}$. In other words, if $j < M$, then j is the unique positive integer in $\{1, 2, \ldots, M\}$ such that $d_{k+1} \leq \sum_{i=1}^{k} d_i + 1$ for all $k = 0, 1, \ldots, j-1$ and $d_{j+1} > \sum_{i=1}^{j} d_i + 1$. On the other hand, if $j = M$, then $d_{k+1} \leq \sum_{i=1}^{k} d_i + 1$ for all $k = 0, 1, \ldots, M-1$. We claim that

$$d \leq \sum_{i=1}^{j} d_i. \quad (5)$$

We prove this claim by contradiction. Suppose that $d \geq \sum_{i=1}^{j} d_i + 1$. Consider the sample path that a packet with delay $\sum_{i=1}^{j} d_i + 1$ initiates a busy period at time t, and there is an arriving packet in every time slot $t+1, t+2, \ldots$. From the monotone and consecutive condition of a linear compressor, we see that the delays for all of the packets after time t are also equal to $\sum_{i=1}^{j} d_i + 1$. Therefore, at time $t_1 = t + \sum_{i=1}^{j} d_i$, there are $\sum_{i=1}^{j} d_i + 1$ packets with delays equal to $\sum_{i=1}^{j} d_i + 1$ stored in the M fibers with delays $d_1, d_2, \ldots, d_M$. If $j = M$, then we have reached a contradiction as the M fibers with delays $d_1, d_2, \ldots, d_M$ can only accommodate a maximum of $\sum_{i=1}^{M} d_i$ packets at each time instance. On the other hand, if $1 \leq j \leq M-1$, then from the fact that the j fibers with delays $d_1, d_2, \ldots, d_j$ can only accommodate a maximum of $\sum_{i=1}^{j} d_i$ packets at each time instance, at least one of the $\sum_{i=1}^{j} d_i + 1$ packets at time t_1 must be stored in one of the $M - j$ fibers with delays $d_{j+1}, d_{j+2}, \ldots, d_M$, and that packet cannot depart at the right time as it has a packet delay $\sum_{i=1}^{j} d_i + 1$ which

is smaller than d_k for all $k \geq j+1$ (this follows from $d_{j+1} > \sum_{i=1}^{j} d_i + 1$ and $d_{j+1} \leq d_{j+2} \leq \cdots \leq d_M$). Again, we have reached a contradiction in this case and the claim is proved.

As $d_1 = 1$ and $d_{k+1} \leq \sum_{i=1}^{k} d_i + 1$ for all $k = 0, 1, \ldots, j-1$, we easily deduce that $d_1 = 1$, $d_2 \leq d_1 + 1 = 2$, $d_3 \leq d_1 + d_2 + 1 \leq 4, \ldots$, and $d_j \leq \sum_{i=1}^{j-1} d_i + 1 \leq 2^{j-1}$. As such, it follows from (5) and $j \leq M$ that

$$d \leq \sum_{i=1}^{j} d_i \leq \sum_{i=1}^{j} 2^{i-1} = 2^j - 1 \leq 2^M - 1.$$

The proof is completed. ■

We note that Theorem 2 immediately shows that the construction in Figure 4 is an optimal construction of a linear compressor among all of the constructions of a linear compressor by using M scaled optical memory cells (there are M fiber delay lines in the M scaled optical memory cells) as the construction in Figure 4 achieves the upper bound $2^M - 1$ on the maximum delay d as prescribed in (3).

The problem with the optimal construction of a linear compressor in Figure 4 is its fault tolerant capability. If one of the scaled optical memory cells does not function properly, then the construction in Figure 4 no longer works. To increase the reliability of the construction via a concatenation of scaled optical memory cells, we assume that each scaled optical memory cell has a bypass circuit. The bypass circuit sets up a direct connection between its input link and its output link once a fault within a scaled optical memory cell is detected. Such a scaled optical memory cell will be called a *fault/bypass* scaled optical memory cell in this paper. Even with fault/bypass scaled optical memory cells, the construction in Figure 4 still does not work when one of the fault/bypass scaled optical memory cells detects a fault.

As we know that a linear compressor with maximum delay $2^M - 1$ can be constructed by a concatenation of M scaled optical memory cells with scaling factors $1, 2, 2^2, \ldots, 2^{M-1}$ as in Figure 4. To construct a linear compressor that can tolerate a failure of a fault/bypass scaled optical memory cell, one may simply use two identical fault/bypass scaled optical memory cells at each stage of the construction as in Figure 5. As such, one can build a linear compressor with maximum delay $2^M - 1$ that can tolerate one faulty scaled optical memory cell by a concatenation of $2M$ scaled optical memory cells with scaling factors $1, 1, 2, 2, \ldots, 2^{M-1}, 2^{M-1}$ by simply using the M functioning scaled optical memory cells with scaling factors $1, 2, \ldots, 2^{M-1}$ and bypassing the other M scaled optical memory cells. In fact, by Theorem 6 in Section IV-A, such a construction in Figure 5 can be operated as a linear compressor with maximum delay $(2^M - 1) + (2^{M-1} - 1)$ in the worst case that can tolerate one faulty scaled optical memory cell (the worst case occurs when the scaled optical memory cell with scaling factor 2^{M-1} is broken). Similarly, one can build a linear compressor with maximum delay $(2^M - 1) + F(2^{M-1} - 1)$ that can tolerate up to F faulty scaled optical memory cells by a concatenation of $(F+1)M$ scaled optical memory cells.

In order to compare various constructions, we introduce the construction efficiency ρ for a construction of a linear compressor. Suppose that a linear compressor with maximum delay d is constructed by using M scaled optical memory cells. Then its construction efficiency ρ is defined to be the ratio of $\log_2(d+1)$ to the number of scaled optical memory cells M used in the construction, i.e.,

$$\rho = \frac{\log_2(d+1)}{M}. \tag{6}$$

The construction efficiency in (6) is defined in such a way that the construction efficiency for an optimal construction with maximum delay $2^M - 1$ is equal to 1 and the construction efficiency for a non-optimal construction with maximum delay less than $2^M - 1$ is less than 1. Note that for a linear compressor constructed by using M scaled optical memory cells that can tolerate F faulty scaled optical memory cells, we use the worst-case maximum delay d in (6) for the calculation of its construction efficiency. As such, the construction efficiency for the direct construction that uses $F+1$ identical scaled optical memory cells at each stage is approximately $1/(F+1)$ if $F << M$, which is much lower than that for the optimal construction in Figure 4. However, the optimal construction in Figure 4 cannot tolerate any failure of scaled optical memory cells. In contrast, the direct construction with a much lower construction efficiency can tolerate up to F failures of scaled optical memory cells.

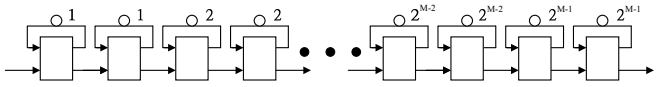


Fig. 5. A direct construction of a fault tolerant linear compressor with maximum delay $(2^M - 1) + (2^{M-1} - 1)$ in the worst case that can tolerate one faulty scaled optical memory cell.

Naturally, the next question we would like to ask is whether there are better constructions than the direct construction that can tolerate up to F failures of scaled optical memory cells and have construction efficiencies greater than $1/(F+1)$? The answer to this question is affirmative and in Section IV we show an optimal construction of a linear compressor that can tolerate up to F faulty scaled optical memory cells and has a construction efficiency greater than $1/(F+1)$. The results in Section IV are made possible by a general construction of a linear compressor given in Section III below.

III. A General Construction of a Linear Compressor

A. A Two-stage Construction of a Linear Compressor

In Figure 6, we consider a two-stage construction of a network element. The first stage is a linear compressor with maximum delay d_1, and the second stage is a scaled linear compressor with maximum delay B and scaling factor d_2. As we have defined in Section II that a scaled SDL element with scaling factor m is an SDL element such that the delay of every delay line in the scaled SDL element is m times of that in the original (unscaled) SDL element, the second stage can be obtained by first constructing an (unscaled) linear compressor with maximum delay B and then increasing the delay of every delay line in the original (unscaled) linear compressor by a

factor of d_2. It should be noted that B is *not* the maximum delay of the scaled linear compressor with maximum delay B and scaling factor d_2 at the second stage in Figure 6. Also note that we have mentioned in Section II that one of the most important properties of SDL elements is the time interleaving property for scaled SDL elements which says that a scaled SDL element with scaling factor m can be operated as the time interleaving of m (unscaled) SDL elements. As such, in the two-stage construction in Figure 6, we will operate the scaled linear compressor with maximum delay B and scaling factor d_2 at the second stage as the time interleaving of d_2 (unscaled) linear compressor with maximum delay B.

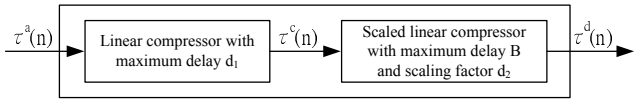


Fig. 6. A two-stage construction of a linear compressor with maximum delay $Bd_2 + d_1$ when $d_2 \leq d_1 + 1$.

In Theorem 3 below, we will show that if $d_2 \leq d_1 + 1$, then such a two-stage construction in Figure 6 can be operated as a linear compressor with maximum delay $Bd_2 + d_1$ under the following operation rule:

(R1) Let $\tau^a(n)$ and $\tau^d(n)$ be the arrival time and the departure time, respectively, of the n^{th} packet for the network element in Figure 6. Note that $\tau^a(n)$ is also the arrival time of the n^{th} packet for the linear compressor with maximum delay d_1 at the first stage, and $\tau^d(n)$ is also the departure time of the n^{th} packet for the scaled linear compressor with maximum delay B and scaling factor d_2 at the second stage. Let $\tau^c(n)$ be the departure time of the n^{th} packet for the linear compressor with maximum delay d_1 at the first stage, which is also the arrival time of the n^{th} packet for the scaled linear compressor with maximum delay B and scaling factor d_2 at the second stage. If $\tau^d(n) - \tau^a(n) \leq Bd_2 - 1$, then we set $\tau^c(n) = \tau^d(n) - d_2\lfloor\frac{\tau^d(n)-\tau^a(n)}{d_2}\rfloor$, namely, $\tau^c(n)$ is given in such a way that the delay of the n^{th} packet at the first stage is $\tau^c(n) - \tau^a(n) = (\tau^d(n) - \tau^a(n)) \bmod d_2$ and the delay of the n^{th} packet at the second stage is $\tau^d(n) - \tau^c(n) = d_2\lfloor\frac{\tau^d(n)-\tau^a(n)}{d_2}\rfloor$. Otherwise, if $\tau^d(n) - \tau^a(n) \geq Bd_2$, then we set $\tau^c(n) = \tau^d(n) - Bd_2$, so that the delay of the n^{th} packet at the first stage is $\tau^c(n) - \tau^a(n) = \tau^d(n) - \tau^a(n) - Bd_2$ and the delay of the n^{th} packet at the second stage is $\tau^d(n) - \tau^c(n) = Bd_2$.

Theorem 3 *Suppose that the two-stage construction in Figure 6 is started from an empty system. If $d_2 \leq d_1 + 1$, then under the operation rule in (R1) the two-stage construction in Figure 6 is a linear compressor with maximum delay $Bd_2 + d_1$.*

Proof. According to Definition 1 for a linear compressor, we need to show that under the operation rule in (R1) the two-stage construction in Figure 6 can realize all of the $\tau^a(n)$ and $\tau^d(n)$ that satisfy the following conditions for all n:

$$\tau^a(n) \leq \tau^d(n) \leq \tau^a(n) + Bd_2 + d_1, \tag{7}$$
$$\tau^d(n) = \tau^d(n-1) + 1 \text{ whenever } \tau^a(n) \leq \tau^d(n-1). \tag{8}$$

It suffices to show that if $\tau^a(n)$ and $\tau^d(n)$ satisfy the conditions in (7) and (8) for all n, then under the operation rule in (R1) they also satisfy the following conditions for all n:

$$\tau^a(n) \leq \tau^c(n) \leq \tau^a(n) + d_1, \tag{9}$$
$$\tau^c(n) = \tau^c(n-1) + 1 \text{ whenever } \tau^a(n) \leq \tau^c(n-1), \tag{10}$$

$$\tau^c(n) \leq \tau^d(n) \leq \tau^c(n) + Bd_2, \tag{11}$$
$$(\tau^d(n) - \tau^c(n)) \bmod d_2 = 0, \tag{12}$$
$$\tau^d(n) = \tau^d(n^*) + d_2 \text{ whenever } \tau^c(n) \leq \tau^d(n^*), \tag{13}$$

where n^* is the last packet (in the busy period containing the n^{th} packet) that departs before the n^{th} packet from the same time interleaved linear compressor at the second stage. If this can be proved, then the set of all $\tau^a(n)$, $\tau^c(n)$, and $\tau^d(n)$ such that $\tau^a(n)$ and $\tau^d(n)$ satisfy the conditions in (7) and (8) and $\tau^c(n)$ is uniquely determined by $\tau^a(n)$ and $\tau^d(n)$ under the operation rule in (R1) for all n is a subset of the set of all $\tau^a(n)$, $\tau^c(n)$, and $\tau^d(n)$ that satisfy the conditions in (9)–(13) for all n as there may exist other $\tau^a(n)$, $\tau^c(n)$, and $\tau^d(n)$ that satisfy the conditions in (9)–(13) for all n. As all of the $\tau^a(n)$ and $\tau^c(n)$ that satisfy the conditions in (9) and (10) for all n can be realized by the linear compressor with maximum delay d_1 at the first stage, and all of the $\tau^c(n)$ and $\tau^d(n)$ that satisfy the conditions in (11)–(13) can be realized by the scaled linear compressor with maximum delay B and scaling factor d_2 at the second stage, it then follows that all of the $\tau^a(n)$, $\tau^c(n)$, and $\tau^d(n)$ such that $\tau^a(n)$ and $\tau^d(n)$ satisfy the conditions in (7) and (8) and $\tau^c(n)$ is uniquely determined by $\tau^a(n)$ and $\tau^d(n)$ under the operation rule in (R1) for all n can be realized by the two-stage construction in Figure 6. In other words, all of the $\tau^a(n)$ and $\tau^d(n)$ that satisfy the conditions in (7) and (8) can be realized by the two-stage construction in Figure 6 under the operation rule in (R1).

In the following, we divide the proof into three parts.

(i) First, we show that (9), (11), and (12) hold for all n. We consider the following two cases:

Case 1: $0 \leq \tau^d(n) - \tau^a(n) \leq Bd_2 - 1$. In this case, we see from (R1) that

$$\tau^c(n) = \tau^d(n) - d_2\left\lfloor\frac{\tau^d(n) - \tau^a(n)}{d_2}\right\rfloor, \tag{14}$$

which implies that

$$\tau^c(n) = \tau^a(n) + ((\tau^d(n) - \tau^a(n)) \bmod d_2). \tag{15}$$

It follows from (15), $\tau^d(n) \geq \tau^a(n)$ in (7), and the assumption $d_2 \leq d_1 + 1$ that

$$\tau^a(n) \leq \tau^c(n) \leq \tau^a(n) + d_2 - 1 \leq \tau^a(n) + d_1.$$

As $0 \leq \lfloor\frac{\tau^d(n)-\tau^a(n)}{d_2}\rfloor \leq B - 1$ in this case, we have from (14) that

$$\tau^c(n) \leq \tau^d(n) \leq \tau^c(n) + (B-1)d_2 \leq \tau^c(n) + Bd_2.$$

Clearly, $(\tau^d(n) - \tau^c(n)) \bmod d_2 = 0$.

Case 2: $Bd_2 \le \tau^d(n) - \tau^a(n) \le Bd_2 + d_1$. In this case, we have from (R1) that $\tau^c(n) = \tau^d(n) - Bd_2$, and it follows that $\tau^a(n) \le \tau^c(n) \le \tau^a(n) + d_1$. Clearly, $\tau^d(n) = \tau^c(n) + Bd_2$ and $((\tau^d(n) - \tau^c(n)) \bmod d_2) = 0$.

(ii) To see that (10) holds, suppose that $\tau^a(n) \le \tau^c(n-1)$. Then we also have $\tau^a(n) \le \tau^d(n-1)$ as $\tau^c(n-1) \le \tau^d(n-1)$ in (11). It follows from (8) that

$$\tau^d(n) = \tau^d(n-1) + 1. \tag{16}$$

Now we consider the following two cases:

Case 1: $(k-1)d_2 \le \tau^d(n-1) - \tau^a(n-1) \le kd_2 - 1,\ k = 1, 2, \ldots, B$. In this case, we see from (R1) that

$$\begin{aligned}\tau^c(n-1) &= \tau^d(n-1) - d_2 \left\lfloor \frac{\tau^d(n-1) - \tau^a(n-1)}{d_2} \right\rfloor \\ &= \tau^d(n-1) - (k-1)d_2. \end{aligned} \tag{17}$$

Using (16), $\tau^a(n) \le \tau^c(n-1)$, and (17) yields

$$\begin{aligned}\tau^d(n) - \tau^a(n) &= \tau^d(n-1) + 1 - \tau^a(n) \\ &\ge \tau^d(n-1) + 1 - \tau^c(n-1) \\ &= (k-1)d_2 + 1.\end{aligned}$$

As $\tau^a(n) > \tau^a(n-1)$, we also have

$$\begin{aligned}\tau^d(n) - \tau^a(n) &= \tau^d(n-1) + 1 - \tau^a(n) \\ &\le \tau^d(n-1) - \tau^a(n-1) \\ &\le kd_2 - 1.\end{aligned}$$

It then follows from (R1) that

$$\begin{aligned}\tau^c(n) &= \tau^d(n) - d_2 \left\lfloor \frac{\tau^d(n) - \tau^a(n)}{d_2} \right\rfloor \\ &= \tau^d(n) - (k-1)d_2. \end{aligned} \tag{18}$$

As a direct result of (18), (17), and (16), we then have

$$\begin{aligned}\tau^c(n) &= \tau^d(n) + \tau^c(n-1) - \tau^d(n-1) \\ &= \tau^c(n-1) + 1.\end{aligned}$$

Case 2: $Bd_2 \le \tau^d(n-1) - \tau^a(n-1) \le Bd_2 + d_1$. In this case, we have from (R1) that

$$\tau^c(n-1) = \tau^d(n-1) - Bd_2. \tag{19}$$

Using (16) and $\tau^a(n) \le \tau^c(n-1)$ yields

$$\begin{aligned}\tau^d(n) &= \tau^d(n-1) + 1 \\ &= \tau^c(n-1) + Bd_2 + 1 \\ &\ge \tau^a(n) + Bd_2 + 1.\end{aligned}$$

From (R1), it follows that

$$\tau^c(n) = \tau^d(n) - Bd_2.$$

In conjunction with (19) and (16), we then have

$$\tau^c(n) = \tau^c(n-1) + 1.$$

(iii) To prove (13), we will show that

$$\tau^d(n) = \tau^d(n^*) + d_2 \text{ whenever } \tau^a(n) \le \tau^d(n^*), \tag{20}$$

which is a stronger result than (13) as we have shown $\tau^a(n) \le \tau^c(n)$ in (9) and hence $\tau^c(n) \le \tau^d(n^*)$ implies that $\tau^a(n) \le \tau^d(n^*)$.

Let $n_0 = \sup\{m \le n : \tau^a(m) > \tau^d(m-1)\}$ be the index of the packet that initiates the busy period containing the n^{th} packet. From (8), it follows that for all $n_0 < m \le n$

$$\tau^d(m) = \tau^d(m-1) + 1. \tag{21}$$

Note that the d_2 time interleaved linear compressors at the second stage are connected to the output link of the linear compressor at the first stage periodically with period d_2. If $n - d_2 \ge n_0$, then $n^* = n - d_2$ is the last packet (in the busy period containing the n^{th} packet) that departs before the n^{th} packet from the same time interleaved linear compressor at the second stage. As such, it follows from (21) that

$$\tau^d(n) = \tau^d(n - d_2) + d_2 = \tau^d(n^*) + d_2.$$

On the other hand, if $n - d_2 < n_0$, then the n^{th} packet arrives at an empty linear compressor at the second stage and there is no need to check (20). ■

We remark that Theorem 3 is a generalization of one of our previous results on the constructions of linear compressors in [21] that holds only for $d_2 = d_1 + 1$ instead of $d_2 \le d_1 + 1$ in Theorem 3. As shown in [21], the condition $d_2 = d_1 + 1$ for the two-stage construction leads to the multistage construction of a linear compressor in Figure 4. However, as we have seen in Section II that such a construction in Figure 4 does not have the fault tolerant capability. In contrast, we will show that the general condition $d_2 \le d_1 + 1$ for the two-stage construction in Theorem 3 also leads to a multistage construction of a linear compressor in Section III-B, which in turn is the key to an optimal construction of a fault tolerant linear compressor in Section IV.

B. A Multistage Construction of a Linear Compressor by a Concatenation of Scaled Optical Memory Cells

As it has been shown in [21] that an optical memory cell can be used as a linear compressor with maximum delay 1, it follows that the network element in Figure 7 is a special case of that in Figure 6 with $B = 1$. As such, it can be operated as a linear compressor with maximum delay $d_1 + d_2$ if $d_2 \le d_1 + 1$.

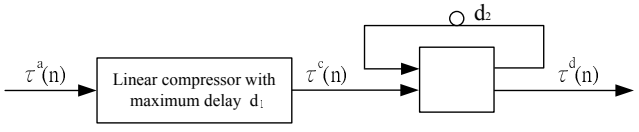


Fig. 7. A two-stage construction of a linear compressor with maximum delay $d_1 + d_2$ when $d_2 \le d_1 + 1$.

Note that if $d_1 = 1$, then the first stage in Figure 7 could be constructed by using an optical memory cell and we have a linear compressor by a concatenation of two scaled optical memory cells. On the other hand, if $d_1 > 1$ in Figure 7, then by recursively expanding the first stage, we obtain a concatenation of M scaled optical memory cells with scaling factors $d_1, d_2, \ldots, d_M$, where $d_1 = 1$ (see Figure 8). Intuitively, with an appropriate choice of the scaling factors

$d_1, d_2, \ldots, d_M$, we expect that the network element in Figure 8 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{M} d_i$.

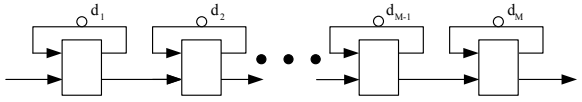


Fig. 8. A multistage construction of a linear compressor by a concatenation of scaled optical memory cells.

In Theorem 4 below, we will show that such a construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M} d_i$ if the delays $d_1, d_2, \ldots, d_M$ are chosen to satisfy the following condition:

(A1) $d_1 = 1$ and $d_k \le d_{k+1} \le \sum_{i=1}^{k} d_i + 1$ for $k = 1, 2, \ldots, M-1$.

To specify the routing in such a construction, let x be the delay of the n^{th} packet, i.e., $x = \tau^d(n) - \tau^a(n)$. For the delay x, we first compute an M-vector $\mathcal{C}(x) = (I_1(x), I_2(x), \ldots, I_M(x))$, where the entries $I_M(x), I_{M-1}(x), \ldots, I_1(x)$, in that order, are given recursively by

$$I_k(x) = \begin{cases} 1, & \text{if } x - \sum_{i=k+1}^{M} I_i(x) d_i \ge d_k, \\ 0, & \text{otherwise.} \end{cases} \tag{22}$$

The M-vector $\mathcal{C}(x) = (I_1(x), I_2(x), \ldots, I_M(x))$ obtained this way is called the $\mathcal{C}$-transform of x with respect to the M-vector $(d_1, d_2, \ldots, d_M)$ in [12], and is a generalization of the well-known binary representation of x (note that the $\mathcal{C}$-transform of x becomes the binary representation of x when $d_k = 2^{k-1}$ for $k = 1, 2, \ldots, M$). The routing of the n^{th} packet is according to the following operation rule:

(R2) Let $\tau_k^d(n)$ be the departure time of the n^{th} packet from the k^{th} stage, $k = 1, 2, \ldots, M-1$. We set

$$\tau_k^d(n) = \tau^d(n) - \sum_{i=k+1}^{M} I_i(x) d_i, \tag{23}$$

for $k = 1, 2, \ldots, M-1$.

It is known from [12] that the $\mathcal{C}$-transform has the unique representation property for all $0 \le x \le \sum_{i=1}^{M} d_i$ under the condition in (A1), i.e.,

$$x = \sum_{i=1}^{M} I_i(x) d_i \text{ for all } x = 0, 1, \ldots, \sum_{i=1}^{M} d_i. \tag{24}$$

As such, if the condition in (A1) holds, then we have from (23), $x = \tau^d(n) - \tau^a(n)$, and (24) that

$$\begin{aligned} \tau_k^d(n) &= \tau^d(n) - \sum_{i=k+1}^{M} I_i(x) d_i \\ &= \tau^a(n) + x - \sum_{i=k+1}^{M} I_i(x) d_i \\ &= \tau^a(n) + \sum_{i=1}^{k} I_i(x) d_i, \end{aligned} \tag{25}$$

for all $k = 1, 2, \ldots, M-1$. In other words, the n^{th} packet is routed to the fiber delay line of the k^{th} scaled optical memory cell if $I_k(x) = 1$.

Theorem 4 *Suppose that the network element in Figure 8 is started from an empty system. If (A1) holds, then under the operation rule in (R2) the construction in Figure 8 is a* self-routing *linear compressor with maximum delay* $\sum_{i=1}^{M} d_i$.

Proof. We first show by induction that the network element consisting of the first k stages in Figure 8 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{k} d_i$ for $k = 1, 2, \ldots, M$. As $d_1 = 1$, this holds trivially for $k = 1$ since an optical memory cell can be used as a linear compressor with maximum delay 1.

Suppose as the induction hypothesis that the network element consisting of the first k stages in Figure 8 is a linear compressor with maximum delay $\sum_{i=1}^{k} d_i$ for some $1 \le k \le M-1$. As the $(k+1)^{th}$ stage is a scaled linear compressor with maximum delay 1 and scaling factor d_{k+1} and $d_{k+1} \le \sum_{i=1}^{k} d_i + 1$, it then follows from Theorem 3 that the network element consisting of the first $k+1$ stages in Figure 8 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{k+1} d_i$ under the operation rule (R1). This completes the induction.

Now we show that the construction in Figure 8 is a self-routing linear compressor with the routing policy specified by (R2). Since the network element consisting of the first $M-1$ stages in Figure 8 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{M-1} d_i$, the construction in Figure 8 is a concatenation of a linear compressor with maximum delay $\sum_{i=1}^{M-1} d_i$ and a scaled linear compressor with maximum delay 1 and scaling factor d_M. As such, the operation rule in (R1) in this case is exactly $\tau_{M-1}^d(n) = \tau^d(n) - I_M(x) d_M$, where x is the delay of the n^{th} packet. Repeating the same argument for $M-1$ times yields

$$\begin{aligned} \tau_k^d(n) &= \tau_{k+1}^d(n) - I_{k+1}(x) d_{k+1} \\ &= \tau^d(n) - \sum_{i=k+1}^{M} I_i(x) d_i \end{aligned}$$

for $k = M-1, M-2, \ldots, 1$. This completes the proof. ■

Example 5 *If we choose* $d_k = 2^{k-1}$ *for* $k = 1, 2, \ldots, M$, *then we have a self-routing linear compressor with maximum delay* $2^M - 1$ *as shown in Figure 4. For this special case, the* $\mathcal{C}$*-transform of* x *is simply the binary representation of* x.

IV. An Optimal Construction of a Fault Tolerant Linear Compressor

A. A General Construction of a Fault Tolerant Linear Compressor

Observe that if $K(F+1) \le M < (K+1)(F+1)$ for some $K \ge 1$, then for the straightforward construction that $d_{(k-1)(F+1)+1} = d_{(k-1)(F+1)+2} = \cdots = d_{k(F+1)} = 2^{k-1}$, $k = 1, 2, \ldots, K$, and $d_{K(F+1)+1} = d_{K(F+1)+2} = \cdots = d_M = 2^K$, the condition in (A1) is still satisfied even after up to F of the M scaled optical memory cells

are broken. As such, the network element in Figure 8 can still be operated as a linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ in the worst case even after up to F of the M scaled optical memory cells detect faults (note that the worst case occurs when the F scaled optical memory cells with scaling factors $d_{M-F+1}, d_{M-F+2}, \ldots, d_M$ are broken). We can easily calculate that the maximum delay in the worst case for such a direct construction is

$$\begin{aligned}\sum_{i=1}^{M-F} d_i &= \sum_{i=1}^{(K-1)(F+1)} d_i + \sum_{i=(K-1)(F+1)+1}^{M-F} d_i \\ &= (F+1)\sum_{k=1}^{K-1} 2^{k-1} + (M-K(F+1)+1)2^{K-1} \\ &= [M-(K-1)(F+1)+1]2^{K-1} - F - 1. \quad (26)\end{aligned}$$

As a result, for $F = 0$, we have $d_i = 2^{i-1}$ for $i = 1, 2, \ldots, M$, and the construction efficiency is equal to 1. For $F \geq 1$, the construction efficiency approaches $\frac{1}{F+1}$ as M tends to infinity, namely, the asymptotic construction efficiency is equal to $\frac{1}{F+1}$. Although the construction efficiency for such a straightforward construction is much smaller than 1 as F becomes large, such a direct construction guarantees that the network element in Figure 8 can still be operated as a linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ in the worst case even after up to F of the M scaled optical memory cells are broken.

In the following theorem, we show how one constructs a linear compressor via fault/bypass scaled optical memory cells that can tolerate up to F faulty scaled optical memory cells and has a construction efficiency greater than $\frac{1}{F+1}$.

Theorem 6 *Let $M \geq 1$ and $0 \leq F \leq M-1$. Suppose that the network element in Figure 8 is started from an empty system and all the scaled optical memory cells in Figure 8 are fault/bypass scaled optical memory cells. If the delays $d_1, d_2, \ldots, d_M$ satisfy the following condition:*

(A2) *$d_k = 1$ for $k = 1, 2, \ldots, F+1$, and $d_k \leq d_{k+1} \leq \sum_{i=1}^{k-F} d_i + 1$ for $k = F+1, F+2, \ldots, M-1$,*

then the construction in Figure 8 can still be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ in the worst case even after up to F of the M scaled optical memory cells detect faults.

Proof. Assume that there are $\tilde{F}$ scaled optical memory cells that detect faults, where $0 \leq \tilde{F} \leq F$. With the bypass circuits, the construction in Figure 8 becomes a concatenation of $M-\tilde{F}$ scaled optical memory cells. Let $\tilde{d}_k$, $k = 1, 2, \ldots, M-\tilde{F}$, be the scaling factor of the k^{th} scaled optical memory cell in the remaining $M-\tilde{F}$ scaled optical memory cells. Clearly, $\tilde{d}_k = d_j$ for some $k \leq j \leq k+\tilde{F}$. As we assume that $d_k \leq d_{k+1}$ for all k in (A2), it follows that

$$d_k \leq \tilde{d}_k \leq d_{k+\tilde{F}}, \quad (27)$$

for all $k = 1, 2, \ldots, M-\tilde{F}$.

Now we show that the delays $\tilde{d}_1, \tilde{d}_2, \ldots, \tilde{d}_{M-\tilde{F}}$ satisfy the condition in (A1). Clearly, $\tilde{d}_k \leq \tilde{d}_{k+1}$ for all $k = 1, 2, \ldots, M-\tilde{F}-1$. As $d_i = 1$ for $i = 1, 2, \ldots, F+1$ and $\tilde{F} \leq F$, we have

$$1 = d_1 \leq \tilde{d}_1 \leq d_{\tilde{F}+1} = 1,$$

implying that $\tilde{d}_1 = 1$. For $1 \leq k \leq F-\tilde{F}$, we have from (27) and $d_i = 1$ for $i = 1, 2, \ldots, F+1$ that

$$\tilde{d}_{k+1} \leq d_{k+1+\tilde{F}} = 1 \leq \sum_{i=1}^{k} \tilde{d}_i + 1.$$

Similarly, for $F-\tilde{F}+1 \leq k \leq M-\tilde{F}-1$, we have from (27), (A2), and $\tilde{F} \leq F$ that

$$\begin{aligned}\tilde{d}_{k+1} \leq d_{k+1+\tilde{F}} &\leq \sum_{i=1}^{k+\tilde{F}-F} d_i + 1 \\ &\leq \sum_{i=1}^{k} d_i + 1 \leq \sum_{i=1}^{k} \tilde{d}_i + 1.\end{aligned}$$

From Theorem 4, the concatenation of the remaining $M-\tilde{F}$ scaled optical memory cells can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-\tilde{F}} \tilde{d}_i$. Since $\tilde{F} \leq F$ and $d_k \leq \tilde{d}_k$ for all k in (27), we have

$$\sum_{i=1}^{M-\tilde{F}} \tilde{d}_i \geq \sum_{i=1}^{M-F} \tilde{d}_i \geq \sum_{i=1}^{M-F} d_i. \quad (28)$$

Note that the inequalities in (28) hold with equality if and only if $\tilde{F} = F$ and $\tilde{d}_k = d_k$ for $k = 1, 2, \ldots, M-F$. In other word, the worst case occurs when the F scaled optical memory cells with the F largest scaling factors $d_{M-F+1}, d_{M-F+2}, \ldots, d_M$ are broken. ■

We note that the condition in (A2) reduces to the condition in (A1) when $F = 0$. As such, the construction of a linear compressor in Figure 8 with the delays $d_1, d_2, \ldots, d_M$ satisfying the condition in (A2) is more general than the construction in Figure 4.

Example 7 *(Generalized Fibonacci sequences) Let $M \geq 1$ and $0 \leq F \leq M-1$. Consider the sequence of fiber delays $d_k = 1$ for all $k = 1, 2, \ldots, F+1$, and $d_{k+1} = d_k + d_{k-F}$ for all $k = F+1, F+2, \ldots, M-1$. We call such a sequence the generalized Fibonacci sequence of order F. Note that when $F = 0$, the generalized Fibonacci sequence reduces to the sequence of powers of 2, i.e., $d_k = 2^{k-1}$ for $k = 1, 2, \ldots, M$. Also note that the well-known Fibonacci sequence is a special case of the generalized Fibonacci sequence with $F = 1$.*

We show that such a sequence of fiber delays satisfy the condition in (A2). Clearly, we have $d_k \leq d_{k+1}$ for all $k = 1, 2, \ldots, M-1$. Now we argue by induction that

$$d_{k+1} = \sum_{i=1}^{k-F} d_i + 1 \quad (29)$$

for all $k = F+1, F+2, \ldots, M-1$. For $k = F+1$, we have $d_{F+2} = d_{F+1} + d_1 = d_1 + 1$ and hence (29) holds for $k =$

$F+1$. *Suppose that (29) holds for some* $F+1 \leq k \leq M-2$ *as the induction hypothesis. Then we have*

$$\begin{aligned} d_{k+2} &= d_{k+1} + d_{k+1-F} \\ &= \sum_{i=1}^{k-F} d_i + 1 + d_{k+1-F} \\ &= \sum_{i=1}^{(k+1)-F} d_i + 1. \end{aligned}$$

Since the Fibonacci sequence grows exponentially at the rate of the golden ratio $(\sqrt{5}+1)/2$*, the efficiency for the construction that uses the Fibonacci sequence as the delays of the fiber delay lines approaches* $\log_2(\frac{\sqrt{5}+1}{2}) = 0.694242$ *as* M *tends to infinity. This is much better than the naive construction that uses two scaled optical memory cells at each stage. In general, the generalized Fibonacci sequence of order* F *grows exponentially at the rate of* r_F*, where* r_F *is the root of the equation* $r^{F+1} - r^F - 1 = 0$ *with the largest magnitude. It follows that its construction efficiency* $\rho_{M,F} = \log_2(\sum_{i=1}^{M-F} d_i + 1)/M = \log_2(d_{M+1})/M$ *approaches the asymptotic construction efficiency* $\rho_F = \log_2(r_F)$ *as* M *tends to infinity. As can be seen from Table I, for* $F \geq 1$ *this is much better than the asymptotic construction efficiency* $1/(F+1)$ *of the naive construction that uses* $(F+1)$ *scaled optical memory cells at each stage.*

F	0	1	2	3	4
$\frac{1}{F+1}$	1	0.5	0.333333	0.25	0.2
ρ_F	1	0.694242	0.551463	0.464958	0.405685
F	5	6	7	8	9
$\frac{1}{F+1}$	0.166667	0.142857	0.125	0.111111	0.1
ρ_F	0.361992	0.328173	0.301066	0.278758	0.260015
F	10	11	12	13	14
$\frac{1}{F+1}$	0.0909091	0.083333	0.076923	0.071429	0.066667
ρ_F	0.244006	0.230142	0.218000	0.207260	0.197682
F	15	16	17	18	19
$\frac{1}{F+1}$	0.0625	0.058824	0.055556	0.052632	0.05
ρ_F	0.189077	0.181297	0.174222	0.167757	0.161822

TABLE I
ASYMPTOTIC CONSTRUCTION EFFICIENCY ρ_F BY USING THE GENERALIZED FIBONACCI SEQUENCE OF ORDER F FOR $0 \leq F \leq 19$.

B. An Optimal Construction of a Fault Tolerant Linear Compressor

In this section, we show that the construction by the generalized Fibonacci sequence of order F in Example 7 is an optimal construction that maximizes the construction efficiency among all of the constructions that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells.

Let $d_k^* = 1$ for $k = 1, 2, \ldots, F+1$, and let

$$d_{k+1}^* = \sum_{i=1}^{k-F} d_i^* + 1 \tag{30}$$

for $k = F+1, F+2, \ldots, M-1$. Let

$$D_{M,F}^* = \sum_{k=1}^{M-F} d_k^*. \tag{31}$$

Theorem 8 *Let* $M \geq 1$ *and* $0 \leq F \leq M-1$*. Consider a linear compressor that is constructed by using* M *scaled optical memory cells. Suppose that it can still be operated as a linear compressor with maximum delay* d *in the worst case after up to* F *of the* M *optical memory cells detect faults. Then* $d \leq D_{M,F}^*$*, where* $D_{M,F}^*$ *is defined in (31).*

Proof. Suppose that there are F scaled optical memory cells that detect faults. Let $\tilde{d}_1 \leq \tilde{d}_2 \leq \cdots \leq \tilde{d}_{M-F}$ be the scaling factors of the remaining $M-F$ scaled optical memory cells, and let $j = \max\{1 \leq j' \leq M-F : \tilde{d}_{k+1} \leq \sum_{i=1}^{k} \tilde{d}_i + 1 \text{ for all } k = 0, 1, \ldots, j'-1\}$. As the remaining scaled optical memory cells can be operated as a linear compressor with maximum delay d in the worst case, by following the same arguments as in the proof of Theorem 2, we have $\tilde{d}_1 = 1$, $\tilde{d}_{k+1} \leq \sum_{i=1}^{k} \tilde{d}_i + 1$ for all $k = 1, 2, \ldots, j-1$, and $d \leq \sum_{i=1}^{j} \tilde{d}_i$.

Let $d_1 \leq d_2 \leq \cdots \leq d_M$ be the scaling factors of the M scaled optical memory cells. Clearly, for all $k = 1, 2, \ldots, M-F$, we have $\tilde{d}_k = d_i$ for some $k \leq i \leq k+F$. As $\tilde{d}_1 = 1$, we must have $d_i = \tilde{d}_1 = 1$ for $i = 1, 2, \ldots, F+1$. For a fixed $1 \leq k \leq j-1$, consider the special case that $\tilde{d}_i = d_i$, $i = 1, \ldots, k$, and $\tilde{d}_{k+1} = d_{k+1+F}$, then from $\tilde{d}_{k+1} \leq \sum_{i=1}^{k} \tilde{d}_i + 1$ we have

$$d_{k+1+F} \leq \sum_{i=1}^{k} d_i + 1. \tag{32}$$

We are now in a position to show that

$$d_i \leq d_i^*, \quad i = 1, 2, \ldots, j+F. \tag{33}$$

We will prove (33) by induction. We already have $d_i = 1 = d_i^*$, $i = 1, 2, \ldots, F+1$. Assume for some $1 \leq k \leq j-1$ that (33) holds for all $i = 1, 2, \ldots, k+F$ as the induction hypothesis. It then follows from (32), the induction hypothesis, and (30) that

$$d_{k+1+F} \leq \sum_{i=1}^{k} d_i + 1 \leq \sum_{i=1}^{k} d_i^* + 1 = d_{k+1+F}^*.$$

Finally, for the special case that $\tilde{d}_i = d_i$, $i = 1, 2, \ldots, M-F$, we have from $d \leq \sum_{i=1}^{j} \tilde{d}_i$, (33), $j \leq M-F$, and (31) that

$$d \leq \sum_{i=1}^{j} \tilde{d}_i = \sum_{i=1}^{j} d_i \leq \sum_{i=1}^{j} d_i^* \leq \sum_{i=1}^{M-F} d_i^* = D_{M,F}^*.$$

The proof is completed. ■

The following corollary follows directly from Theorem 8 and Example 7.

Corollary 9 *The asymptotic construction efficiency for a linear compressor that can tolerate up to* F *faulty optical memory cells by using* M *scaled optical memory cells is bounded above by* $\rho_F = \log_2(r_F)$*, where* r_F *is the root of the equation* $r^{F+1} - r^F - 1 = 0$ *with the largest magnitude.*

V. An Optimal Construction of a Fault Tolerant Linear Decompressor

The mirror image of an SDL element is an SDL element that reverses the direction of every link in the original SDL element. By so doing, the inputs (resp. outputs) of the original SDL element become the outputs (resp. inputs) of its mirror image. It is obvious that if a sample path can be realized by an SDL element, then its time reversed sample path can also be realized by the mirror image of the SDL element

The mirror image of a linear compressor is called a linear decompressor in [21] as defined below.

Definition 10 (Linear decompressors [21]) *Suppose that the departure time of a packet is known upon its arrival. Let $\tau^a(n)$ and $\tau^d(n)$ be the arrival time and the departure time, respectively, of the n^{th} packet. A network element with a single input link and a single output link is called a* linear decompressor *with the range of delay $[d_1, d_2]$ if it realizes the set of mappings that satisfy (1), the FIFO condition: $\tau^d(n-1) < \tau^d(n)$ for all n, and the following* inverse *monotone and consecutive condition: $\tau^a(n) = \tau^a(n-1) + 1$ whenever $\tau^a(n) \leq \tau^d(n-1)$. In particular, if $d_1 = 0$, then it is called a linear decompressor with maximum delay d_2.*

Suppose a linear decompressor with maximum delay d is constructed by using M scaled optical memory cells. As for a linear compressor, its construction efficiency ρ is defined as

$$\rho = \frac{\log_2(d+1)}{M}. \tag{34}$$

As a linear decompressor is the mirror image of a linear compressor, the construction in Figure 8 can be operated as a linear decompressor and the optimal construction efficiency is achieved by the generalized Fiboncacci sequence as stated in the following theorem and its corollary.

Theorem 11 *Let $M \geq 1$ and $0 \leq F \leq M-1$. Suppose that the network element in Figure 8 is started from an empty system and all the scaled optical memory cells in Figure 8 are fault/bypass scaled optical memory cells. Let $d'_k = d_{M+1-k}$ for $k = 1, 2, \ldots, M$. If $d'_k = 1$ for $k = 1, 2, \ldots, F+1$, and*

$$d'_k \leq d'_{k+1} \leq \sum_{i=1}^{k-F} d'_i + 1 \tag{35}$$

for $k = F+1, F+2, \ldots, M-1$, then the construction in Figure 8 can still be operated as a self-routing linear decompressor with maximum delay $\sum_{i=1}^{M-F} d'_i$ in the worst case even after up to F of the M scaled optical memory cells detect faults.

Conversely, consider a linear decompressor that is constructed by using M scaled optical memory cells. Suppose that it can still be operated as a linear decompressor with maximum delay d in the worst case after up to F of the M scaled optical memory cells detect faults. Then $d \leq D^*_{M,F}$, where $D^*_{M,F}$ is defined in (31).

Corollary 12 *The asymptotic construction efficiency for a linear decompressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells is bounded above by $\rho_F = \log_2(r_F)$, where r_F is the root of the equation $r^{F+1} - r^F - 1 = 0$ with the largest magnitude.*

VI. Conclusion

In this paper, we considered SDL constructions of fault tolerant linear compressors and linear decompressors. The basic network element for our constructions is scaled optical memory cell, which is constructed by a 2×2 optical crossbar switch and a fiber delay line. Such consideration of fault tolerant capability is extremely important and challenging from a practical point of view as otherwise the linear compressors and linear decompressors may fail to function properly even when a single scaled optical memory cell is broken.

We first obtained a fundamental result on the minimum construction complexity of a linear compressor by using fiber delay lines as the storage devices for the packets queued in the linear compressor. This result shows that one of our previous constructions of a linear compressor by a concatenation of scaled optical memory cells is an optimal construction in the sense of minimizing the construction complexity. However, such an optimal construction lacks the fault tolerant capability. To construct a linear compressor with fault tolerant capability, we provided a two-stage construction of a linear compressor. Such a two-stage construction was then recursively expanded to give a multistage construction of a self-routing linear compressor by a concatenation of scaled optical memory cells. We have shown that if the delays $d_1, d_2, \ldots, d_M$ satisfy the condition in (A1), then our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M} d_i$. We have also shown a more general result that if the delays $d_1, d_2, \ldots, d_M$ satisfy the condition in (A2), then our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ in the worst case even after up to F of the M scaled optical memory cells are broken. Furthermore, we have proved that our multistage construction with the delays $d_1, d_2, \ldots, d_M$ given by the generalized Fibonacci sequence of order F is the best among all of the constructions of a linear compressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells. Similar results were also obtained for the constructions of fault tolerant linear decompressors.

Finally, we note that a recent work on the constructions of fault tolerant optical 2-to-1 FIFO multiplexers by one of the authors can be found in [14].

References

[1] M. J. Karol, "Shared-memory optical packet (ATM) switch," in *Proceedings SPIE : Multigigabit Fiber Communication Systems (1993)*, October 1993, vol. 2024, pp. 212–222.

[2] Z. Hass, "The "staggering switch": An electronically controlled optical packet switch," *IEEE Journal of Lightwave Technology*, vol. 11, pp. 925–936, May/June 1993.

[3] I. Chlamtac and A. Fumagalli, "Quadro-star: A high performance optical WDM star network," *IEEE Transactions on Communications*, vol. 42, pp. 2582–2591, August 1994.

[4] I. Chlamtac, A. Fumagalli, L. G. Kazovsky, P. Melman, W. H. Nelson, P. Poggiolini, M. Cerisola, A. N. M. M. Choudhury, T. K. Fong, R. T. Hofmeister, C.-L. Lu, A. Mekkittikul, D. J. M. Sabido IX, C.-J. Suh, and E. W. M. Wong, "Cord: contention resolution by delay lines," *IEEE Journal on Selected Areas in Communications*, vol. 14, pp. 1014–1029, June 1996.

[5] R. L. Cruz and J.-T. Tsai, "COD: alternative architectures for high speed packet switching," *IEEE/ACM Transactions on Networking*, vol. 4, pp. 11–21, February 1996.

[6] D. K. Hunter, D. Cotter, R. B. Ahmad, D. Cornwell, T. H. Gilfedder, P. J. Legg, and I. Andonovic, "2×2 buffered switch fabrics for traffic routing, merging and shaping in photonic cell networks," *IEEE Journal of Lightwave Technology*, vol. 15, pp. 86–101, January 1997.

[7] D. K. Hunter, W. D. Cornwell, T. H. Gilfedder, A. Franzen, and I. Andonovic, "SLOB: a switch with large optical buffers for packet switching," *IEEE Journal of Lightwave Technology*, vol. 16, pp. 1725–1736, October 1998.

[8] E. Varvarigos, "The "packing" and the "scheduling packet" switch architectures for almost all-optical lossless networks," *IEEE Journal of Lightwave Technology*, vol. 16, pp. 1757–1767, October 1998.

[9] I. Chlamtac, A. Fumagalli, and C.-J. Suh, "Multibuffer delay line architectures for efficient contention resolution in optical switching nodes," *IEEE Transactions on Communications*, vol. 48, pp. 2089–2098, December 2000.

[10] C.-S. Chang, D.-S. Lee, and C.-K. Tu, "Recursive construction of FIFO optical multiplexers with switched delay lines," *IEEE Transactions on Information Theory*, vol. 50, pp. 3221–3233, December 2004.

[11] C.-S. Chang, D.-S. Lee, and C.-K. Tu, "Using switched delay lines for exact emulation of FIFO multiplexers with variable length bursts," *IEEE Journal on Selected Areas in Communications*, vol. 24, pp. 108–117, April 2006.

[12] C.-C. Chou, C.-S. Chang, D.-S. Lee and J. Cheng, "A necessary and sufficient condition for the construction of 2-to-1 optical FIFO multiplexers by a single crossbar switch and fiber delay lines," *IEEE Transactions on Information Theory*, vol. 52, pp. 4519–4531, October 2006.

[13] Y.-T. Chen, C.-S. Chang, J. Cheng, and D.-S. Lee, "Feedforward SDL constructions of output-buffered multiplexers and switches with variable length bursts," in *Proceedings IEEE International Conference on Computer Communications (INFOCOM'07)*, Anchorage, AK, USA, May 6–12, 2007.

[14] J. Cheng, "Constructions of fault tolerant optical 2-to-1 FIFO multiplexers," *IEEE Transactions on Information Theory*, vol. 53, pp. 4092–4105, November 2007.

[15] J. Cheng, "Constructions of optical 2-to-1 FIFO multiplexers with a limited number of recirculations," *IEEE Transactions on Information Theory*, vol. 54, September 2007.

[16] C.-S. Chang, Y.-T. Chen, and D.-S. Lee, "Constructions of optical FIFO queues," *IEEE Transactions on Information Theory*, vol. 52, pp. 2838–2843, June 2006.

[17] P.-K. Huang, C.-S. Chang, J. Cheng, and D.-S. Lee, "Recursive constructions of parallel FIFO and LIFO queues with switched delay lines," *IEEE Transactions on Information Theory*, vol. 53, pp. 1778–1798, May 2007.

[18] A. D. Sarwate and V. Anantharam, "Exact emulation of a priority queue with a switch and delay lines," *Queueing Systems: Theory and Applications*, vol. 53, pp. 115–125, July 2006.

[19] H.-C. Chiu, C.-S. Chang, J. Cheng, and D.-S. Lee, "A simple proof for the constructions of optical priority queues," *Queueing Systems: Theory and Applications*, vol. 56, pp. 73–77, June 2007

[20] H.-C. Chiu, C.-S. Chang, J. Cheng, and D.-S. Lee, "Using a single switch with $O(M)$ inputs/outputs for the construction of an optical priority queue with $O(M^3)$ buffer," in *Proceedings IEEE International Conference on Computer Communications (INFOCOM'07 Minisymposium)*, Anchorage, AK, USA, May 6–12, 2007.

[21] C.-S. Chang, Y.-T. Chen, J. Cheng, and D.-S. Lee, "Multistage constructions of linear compressors, non-overtaking delay lines, and flexible delay lines," in *Proceedings IEEE International Conference on Computer Communications (INFOCOM'06)*, Barcelona, Spain, April 23–29, 2006.

[22] T.-H. Chao, C.-S. Chang, D.-S. Lee, and J. Cheng, "Constructions of multicast flexible delay lines and optical multicast switches with 100% throughput," in *Proceedings IEEE Global Telecommunications Conference (GLOBECOM'07)*, Washington DC, USA, November 26–30, 2007.

[23] J. Cheng, C.-S. Chang, T.-H. Chao, D.-S. Lee, and C.-M. Lien, "On constructions of optical queues with a limited number of recirculations," in *Proceedings IEEE International Conference on Computer Communications (INFOCOM'08)*, Phoenix, AZ, USA, April 13–18, 2008.

[24] D.-S. Lee, C.-S. Chang, J. Cheng, and H.-S. Yan, "Queueing analysis of loss systems with variable optical delay lines," in *Proceedings IEEE International Conference on Computer Communications (INFOCOM'08)*, Phoenix, AZ, USA, April 13–18, 2008.

[25] H.-W. Lan, C.-S. Chang, J. Cheng, and D.-S. Lee, "Constructions and analysis of crosstalk-free optical queues," in *Proceedings IEEE International Conference on High Performance Switching and Routing (HPSR'08)*, Shanghai, China, May 15–17, 2008.

[26] S.-Y. R. Li and X.-J. Tan, "Fiber memory," submitted to *IEEE Transactions on Information Theory*.

[27] D. K. Hunter, M. C. Chia, and I. Andonovic, "Buffering in optical packet switches," *IEEE Journal of Lightwave Technology*, vol. 16, pp. 2081–2094, December 1998.

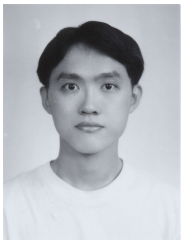
[28] S. Yao, B. Mukherjee, and S. Dixit, "Advances in photonic packet switching: An overview," *IEEE Communications Magazine*, vol. 38, pp. 84–94, February 2000.

[29] D. K. Hunter and I. Andonovic, "Approaches to optical Internet packet switching," *IEEE Communications Magazine*, vol. 38, pp. 116–122, September 2000.

[30] J. Hui, *Switching and Traffic Theory for Integrated Broadband Networks*, Boston, MA: Kluwer Academic Publishers, 1990.

[31] S.-Y. R. Li, *Algebraic Switching Theory and Broadband Applications*, San Diego, CA: Academic Press, 2001.

Cheng-Shang Chang (S'85-M'86-M'89-SM'93-F'04) received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1983, and the M.S. and Ph.D. degrees from Columbia University, New York, NY, USA, in 1986 and 1989, respectively, all in Electrical Engineering. From 1989 to 1993, he was a Research Staff Member at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA. Since 1993, he has been with the Department of Electrical Engineering at National Tsing Hua University, Hsinchu, Taiwan, R.O.C., where he is a currently Professor. His current research interests are in high speed switching, communication network theory, and mathematical modeling of the Internet. Dr. Chang received an IBM Outstanding Innovation Award in 1992, an IBM Faculty Partnership Award in 2001, and Outstanding Research Awards from the National Science Council, Taiwan, in 1998, 2000 and 2002, respectively. He also received Outstanding Teaching Awards from both the college of EECS and the university itself in 2003. He was appointed as the first Y. Z. Hsu Scientific Chair Professor in 2002. He is the author of the book "Performance Guarantees in Communication Networks." and the coauthor of the book "Principles, Architectures and Mathematical Theory of High Performance Packet Switches." He served as an editor for Operations Research from 1992 to 1999. Dr. Chang is a member of IFIP Working Group 7.3 and an editor for IEEE/ACM Transactions on Networking.



Jay Cheng (S'00-M'03) received the B.S. and M.S. degrees from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1993 and 1995, respectively, and the Ph.D. degree from Cornell University, Ithaca, NY, USA, in 2003, all in Electrical Engineering. In August 2003, he joined the Department of Electrical Engineering at National Tsing Hua University, Hsinchu, Taiwan, R.O.C., where he is currently an Associate Professor. Since October 2004, he has also been affiliated with the Institute of Communications Engineering at National Tsing Hua University, Hsinchu, Taiwan, R.O.C. He received the fifth "Y. Z. Hsu Scientific Paper Award" bestowed by Far Eastern Y. Z. Hsu Science and Technology Memorial Foundation in 2007. His current research interests include optical queueing theory, switching theory, communications theory, and information theory.

Tsz-Hsuan Chao (S'00) received the B.S. degree in Mathematics from National Taiwan University, Taipei, Taiwan, R.O.C., in 1998, and the M.S. degree in Electrical Engineering from Chung Hua University, Hsinchu, Taiwan, R.O.C., in 2003. She is currently pursuing her Ph.D. degree at the Institute of Communications Engineering, National Tsing Hua University, Hsinchu, Taiwan, R.O.C. Her current research interests include optical queueing theory, switching theory, and communications network theory.

Duan-Shin Lee (S'89-M'90-SM'98) received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1983, and the MS and Ph.D. degrees from Columbia University, New York, NY, USA, in 1987 and 1990, respectively, all in Electrical Engineering. He was a research staff member at the C&C Research Laboratory of NEC USA, Inc., Princeton, NJ, USA, from 1990 to 1998. He joined the Department of Computer Science at National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1998, where he is currently a Professor. He received the fourth "Y. Z. Hsu Scientific Paper Award" bestowed by Far Eastern Y. Z. Hsu Science and Technology Memorial Foundation in 2006. His research interests are in high-speed switch and router design, wireless networks, performance analysis of communication networks, and queueing theory.